U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

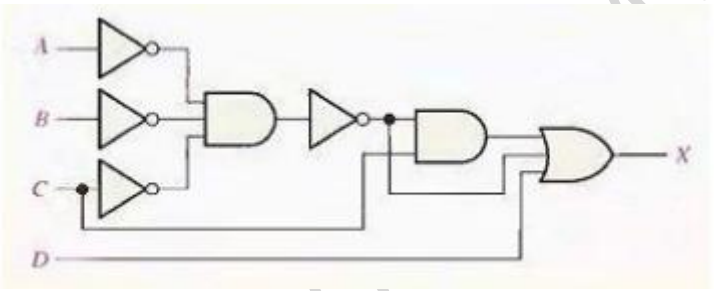
Programme: B.E. **Semester: III**

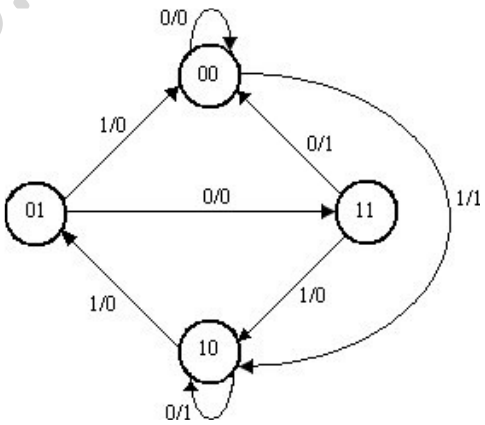
Branch: ES CLUSTER (EC/EE/EI/ML/ET) **Duration: 3 hrs.**

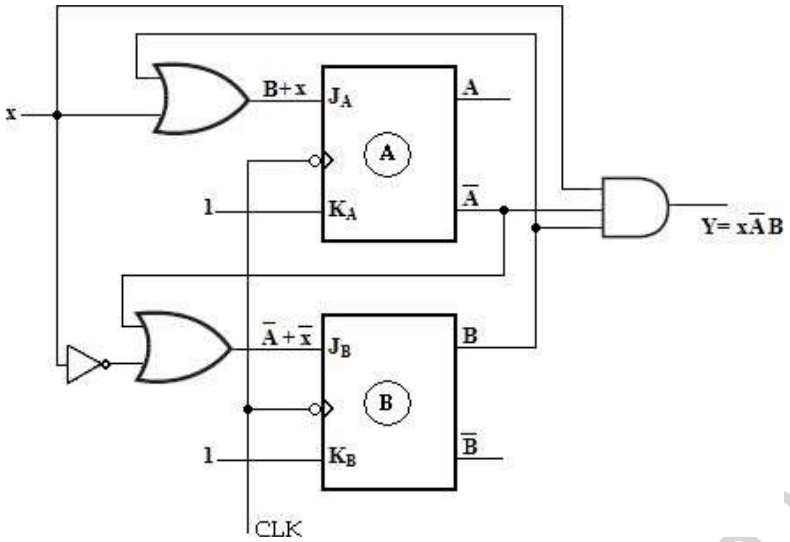
Course Code: 19ES3CCDEC **Max Marks: 100**

Course: Digital Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	CO	PO	Marks
1	a)	Reduce the following circuit to minimal form 	CO1	PO2	**06**
	b)	Determine the simplified form for the function USING k-Map $F(a,b,c,d) = \sum m(0,2,4,7,8,10,12)$. Realize the simplified expression using logic gates with SOP and POS form.	CO1	PO2	**14**
		OR			
2	a)	Design a logic circuit having 3 inputs, A, B, C will have its output HIGH only when a majority of the inputs are HIGH.	CO1	PO2	**10**
	b)	Simplify using tabulation method $F(A,B,C,D) = \sum m(2,3,7,9,11,13) + \sum dc(1,10,15)$	CO1	PO2	**10**
		UNIT - II			
3	a)	Design a 3 bit carry look ahead adder circuit.	CO2	PO3	**10**
	b)	A combinational circuit is defined by the functions $F_1(A,B,C) = \sum m(3,5,6,7)$ $F2 = (A,B,C) = \sum m(0,2,4,7)$ Implement the circuit with a PLA having three inputs, four product terms and two outputs.	CO2	PO3	**10**

			OR			
	4	a)	Implement the following Boolean function with a 4:1 Mux with yz as select inputs $f(w,x,y,z) = \sum m(1,3,4,11,12,14,15)$	*CO2*	*PO3*	**10**
		b)	Consider a 4-bit adder circuit. Design a circuit that will convert the adder to a binary coded decimal form.	*CO2*	*PO3*	**10**
			UNIT - III			
	5	a)	Draw the circuit of JK master slave flipflop and explain when the input is 10 and 11. Show the timing diagram for the same.	*CO3*	*PO3*	**08**
		b)	Design a 4-bit ripple down counter using T flipflops.	*CO3*	*PO3*	**06**
		c)	Design a shift register using multiplexers and D flipflops to perform the following operations. S1 S0 operation 0 0 Circular right shift 0 1 Hold 1 0 Left shift 1 1 Parallel load	*CO3*	*PO3*	**06**
			OR			
	6	a)	Convert JK to D, JK to SR flip flop	*CO3*	*PO3*	**08**
		b)	Design a 3-bit synchronous counter to count the sequence 0,2,4,6. The unused states should reset the counter to zero. Use T flipflop	*CO3*	*PO3*	**12**
			UNIT - IV			
	7	a)	Define FSM.Differentiate between Mealy and Moore models.	*CO3*	*PO3*	**08**
		b)	A sequential circuit has one input and one output. The state diagram is shown below. Design the sequential circuit with D-Flip-Flops 	*CO3*	*PO3*	**12**

			OR			
	8	a)	Determine the state table and state diagram for the circuit shown 	*CO3*	*PO3*	**10**
		b)	Design a Mealy state diagram to detect the sequence "101" for both overlapping and non-overlapping methods.	*CO3*	*PO3*	**10**
			UNIT - V			
	9	a)	Explain the terms i) Rise time and fall time ii) Propagation delay iii) Noise Margin	*CO1*	*PO2*	**08**
		b)	Explain the standard TTL logic circuit and explain its operation	*CO1*	*PO2*	**08**
		c)	Draw the circuit of CMOS NOT gate	*CO1*	*PO2*	**04**
			OR			
	10	a)	Compare TTL and CMOS ICs in terms of characteristics	*CO1*	*PO2*	**08**
		b)	Draw the circuit of CMOS NAND gate explain with truth table	*CO1*	*PO2*	**08**
		c)	A NAND gate has the following characteristics. $I_{OH}(max) = 2$ mA $I_{OL}(max) = 20$ mA $I_{IH}(max) = 20$ μA $I_{IL}(max) = 0.5$ mA Determine fanout for high and low state.	*CO1*	*PO2*	**04**

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