U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: ES CLUSTER(ECE/EE/ML/ET/EI) **Duration: 3 hrs.**
Course Code: 19ES3CCDEC **Max Marks: 100**
Course: Digital Electronic Circuits **Date: 12.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Simplify the Boolean function f(a,b,c,d) = Σ(0,1,2,3,8,9) using Tabulation method.	**08**
	b)	Implement XOR gate using only NOR gates.	**04**
	c)	Simplify the following expression using K-map and realize the logic using only NAND gates. f(A,B,C,D) = Σm(2,3,4,5,13,15) + Σd(8,9,10,11)	**08**

UNIT - II

2	a)	Explain the operation of Carry look ahead adder with relevant logic diagram and equations.	**08**
	b)	Explain the operation of 3 to 8 line decoder.	**06**
	c)	Implement the Boolean expression f(a,b,c) = Σ(1,4,5,7) using 4:1 Multiplexer.	**06**

OR

3	a)	Design a two bit magnitude comparator and implement with suitable logic gates.	**10**
	b)	Write Short notes on (i) Read Only Memories (ROMs) (ii) Programmable Logic Arrays (PLAs).	**10**

UNIT - III

4	a)	What is a flip-flop? Explain the operation of clocked RS flip-flop.	**06**
	b)	Explain the operation of Master-Slave JK flip-flop.	**06**
	c)	Convert the following (i) SR flip-flop to D flip-flop (ii) JK flip-flop to T flip-flop.	**08**

OR

5	a)	Explain the SISO Shift register operations with suitable logic diagram.	**06**
	b)	Design a Modulo 6 ripple counter using T flip-flops.	**07**
	c)	Design a synchronous Modulo 6 counter using D-flip-flops to generate the sequence (0, 2, 3, 5, 6, 1, 0…..)	**07**

UNIT - IV

6 a) Analyze the Moore sequential circuit shown in fig.1 and construct the transition table, State table and State diagram. **12**

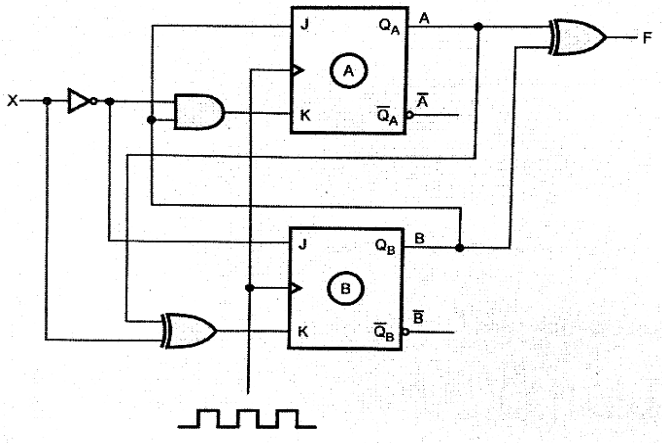

fig.1

b) Design the sequential circuit using D-flip-flops for the state diagram of the sequential circuit shown in figure 2 which has one input and one output. **08**

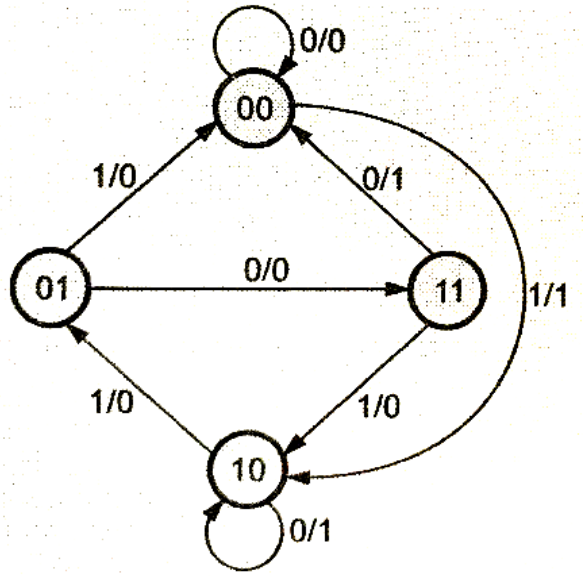

figure 2

UNIT - V

7 a) With a neat circuit diagram explain the operation of two input TTL NAND gate. **06**

b) With neat diagrams explain the operation of (i) CMOS NAND Gate (ii) CMOS NOR gate. **08**

c) Compare TTL and CMOS logic families. **06**

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