U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

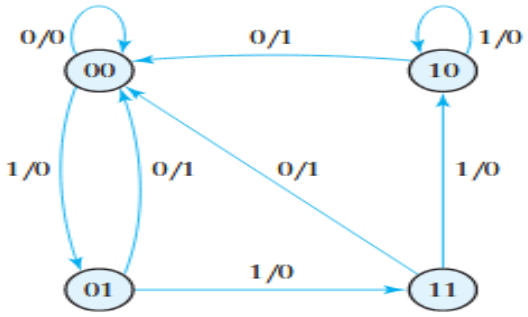
June / July 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: III**
Branch: ES Cluster (EEE/ET/ECE/EIE/MD) **Duration: 3 hrs.**
Course Code: 23ES3PCDEC **Max Marks: 100**
Course: Digital Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

				CO	*PO*	Marks
			UNIT - I			
1	a)		Using Karnaugh maps,determine all the prime implicants and prime implicates for the function f given by f(a,b,c,d)=∏(1,2,3,4,9,10)+∏d(0,14,15).Find the minimal sum to realize f using only NAND gates.	*CO1*	*PO1*	**10**
	b)		Using Quine Mc-Cluskey's Method,obtain a mimimal sum for the boolean function F given by F(a,b,c,d)=Σm(2,3,7,9,11,13)+Σd(1,10,15).	*CO1*	*PO1*	**10**
			UNIT - II			
2	a)		Design and implement a 4-bit look ahead carry adder. How is it advantageous over Binary ripple adder.	*CO2*	*PO2*	**10**
	b)		Design a binary to gray converter for a 4-bit number.	*CO2*	*PO2*	**10**
			OR			
3	a)		Realize the Boolean functions f1(x,y,z)=Σm(0,1,3,5) and f2(x,y,z)=Σm(3,5,7) using a 3x4x2 PLA.Write the PLA table.	*CO2*	*PO2*	**10**
	b)		Design a system to accept a 4 bit input ABCD and generate an output whenever the input code is divisible by either 3 or 5 and represent the output using 4:1 multiplexer.Take C,D as select lines.	*CO2*	*PO2*	**10**
			UNIT - III			
4	a)		Convert i) JK flip-flop to SR Flip-flop ii) D flip-flop to T flip-flop	*CO2*	*PO2*	**10**
	b)		Design a synchronous Mod-6 counter with the following sequence 0,2,3,6,5,1,0……., and repeat.Use D flip-flops.	*CO3*	*PO3*	**10**
			OR			

	5	a)	Draw a 4-bit shift register using D flip-flops.Show how it can be used as a ring and twisted ring counter.	*CO2*	*PO2*	**06**
		b)	Design a counter using T flip-flops with the following binary sequence 0,4,2,1,6 and repeat.	*CO3*	*PO3*	**10**
		c)	Derive the characteristic equation for T flip-flop.	*CO2*	*PO2*	**04**
			UNIT - IV			
	6	a)	Design a synchronous circuit using positive edge triggered JK flip-flops with minimal combinational gating to generate the following sequence. 0-1-2-0 if the input X=0 and 0-2-1-0 if the input X=1 Provide an output which goes high to indicate non-zero states in the 0-1-2-0 sequence.	*CO3*	*PO3*	**10**
		b)	Design a sequential circuit for the following state diagram using JKFF 	*CO3*	*PO3*	**10**
			UNIT - V			
	7	a)	Implement CMOS NOT, NAND and NOR gates.	*CO1*	*PO1*	**10**
		b)	Explain any five characteristics of Digital ICs.	*CO1*	*PO1*	**10**

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