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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

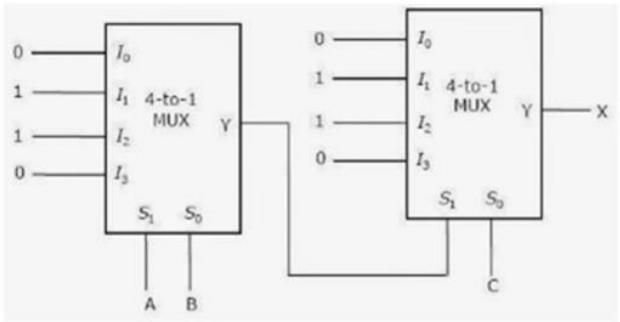
Branch: EEE/ETE/EIE/MD **Duration: 3 hrs.**

Course Code: 23ES3PCDEC **Max Marks: 100**

Course: Digital Electronic Circuits

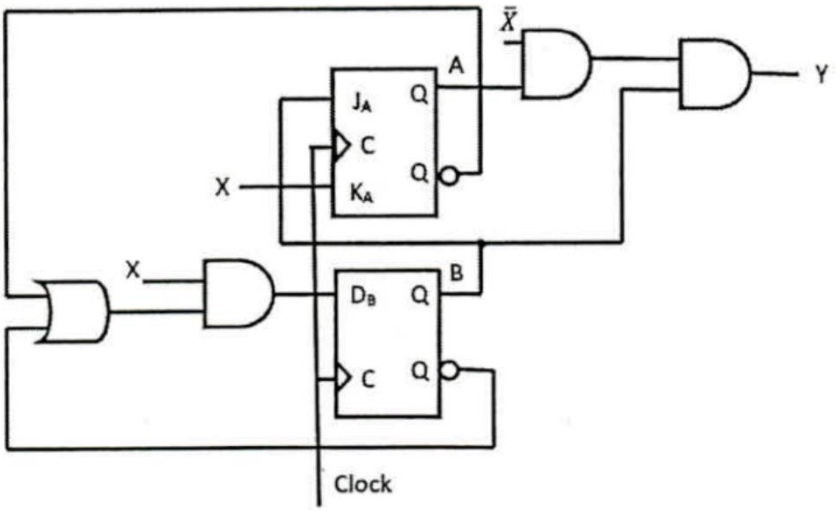
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

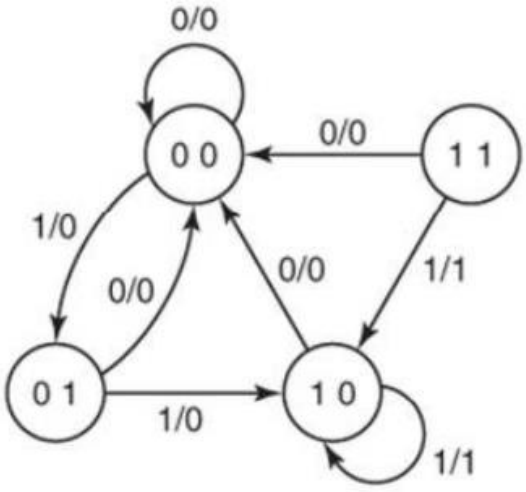
		UNIT - I	CO	PO	Marks
1	a)	ISRO consists of four computers out of which two are connected to the space craft at any given time and remaining two computers are used to ensure safety operation in case if any one fails. Design a low-cost logic circuit which sends a warning signal if two or more computers fail. ("HIGH" signal indicate a working computer, while "LOW" signal indicate a failing computer).	CO1	PO3	**06**
	b)	Simplify the function f (A, B, C, D) = ABC + AB +A'BC'D' + BC' using Karnaugh map.	CO1	PO2	**06**
	c)	Simplify the following switching function using tabular method and identify the Prime implicants and essential prime implicants f (p,q,r,s) = Σm (4,5,8,9,12,13) + Σd (0,3,7,10,11)	CO1	PO2	**08**
		OR			
2	a)	Find the minimized expression for the following function using tabular method F(W,X,Y,Z) = Σm(0,3,5,6,7,10,12,13) + Σd(2,9,15).	CO1	PO3	**10**
	b)	Simplify the following expression using K-map. F(W,X,Y,Z)=ΠM(0,3,4,7,8,10,12,14))+ Πd(2,6).	CO1	PO2	**05**
	c)	Three input variables A, B and C are available. The output is equal to '1' if the input variables have more 1's than 0's. The output is '0' otherwise. Derive the expression and write the circuit for the same.	CO1	PO2	**05**
		UNIT - II			
3	a)	Implement the following functions using a 3x4x2 PLA, with both true and complemented outputs: f1(a,b,c)=∑m(0,1,3,5) f2(a,b,c)=∑m(0,2,3,4)	CO2	PO3	**08**
	b)	Design 2-Bit Magnitude comparator	CO2	PO3	**08**

		c)	Implement binary full substractor using 3:8 decoder	*CO2*	*PO3*	**04**
			OR			
	4	a)	Design a single digit BCD adder to add given two decimal numbers.	*CO2*	*PO3*	**08**
		b)	Analyse the circuit shown in Figure 2b, find the expression for X and also write the truth table.  Figure 2b.	*CO2*	*PO3*	**04**
		c)	Design a 4 bit Binary to Grey Code Converter	*CO2*	*PO3*	**08**
			UNIT - III			
	5	a)	Explain the working of JK M/S flip flop with the help of a neat diagram & waveforms.	*CO3*	*PO2*	**10**
		b)	Design a 4 bit shift register using edge triggered D flip-flops to operate as indicated in the table below Mode | Register Operation 0 0 Hold(No Change) 0 1 Shift Right 1 0 Shift Left 1 1 Parallel	*CO3*	*PO3*	**10**
			OR			
	6	a)	An PN flip -flop has four operations: complement, set to 1, clear to 0 and no change when inputs P and N are 00, 01, 10, and 11 respectively. i. Tabulate the characteristic table , ii. Derive the characteristic equation. iii. Tabulate the excitation table. iv. Show how the JK flip-flop can be converted to a PN flip-flop.	*CO3*	*PO3*	**10**
		b)	Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop. Is the counter self-starting?	*CO3*	*PO3*	**10**

			UNIT - IV			
	7	a)	Design the following state machine using TFF. Write state diagram and State table. The machine is of a single input and single output type. Assume A=00, B=01, C=10, D=11.	*CO3*	*PO3*	**10**
		b)	Analyze the synchronous sequential circuit shown below. Obtain its state table and state diagram. Identify the machine.	*CO3*	*PO3*	**10**
			OR			
	8	a)	Design a Mealy Model for the sequence 1101 with non-overlapping condition using D- flip flops.	*CO3*	*PO3*	**10**
		b)	Construct the excitation table, transition table, state table and sequential circuit with T-Flip flops for the following state diagram.	*CO3*	*PO3*	**10**

Present State	Next State		Output Z	
	X=0	X=1	X=0	X=1
A	B	C	0	0
B	A	A	0	1
C	D	A	0	1
D	A	D	0	1





			UNIT - V			
	9	a)	Explain the following characteristics for digital IC's: i. Noise Margin ii. Propagation delay iii. Power dissipation iv. Fan-out	*CO2*	*PO1*	**10**
		b)	Design and explain the operation of CMOS 2 input NAND and NOR gates.	*CO2*	*PO1*	**10**
			OR			
	10	a)	Explain the working of a TTL NAND gate with the help of a neat circuit diagram.	*CO2*	*PO1*	**10**
		b)	Suppose, for a family of logic components, VIL is 0.6V and VIH is 1.2V. What voltages are required for VOL and VOH to provide a noise margin of 0.2V	*CO2*	*PO1*	**05**
		c)	Make a comparison between TTL and CMOS families with respect to some parameters	*CO2*	*PO1*	**05**

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