U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: EEE/ETE/EIE/MD **Duration: 3 hrs.**

Course Code: 23ES3PCDEC **Max Marks: 100**

Course: Digital Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

				CO	PO	Marks
			UNIT - I			
1	a)		Simplify the Boolean function using K-map and write the circuit diagram for the same. $F(w, x, y, z) = \sum m(1, 3, 7, 11, 15) + \sum d(0,2,5)$	CO1	PO2	**05**
	b)		Simplify the Boolean function $F(A,B,C,D) = \sum m(1,5,6,12,13,14) + \sum d(2,4)$ using Tabular method.	CO1	PO2	**10**
	c)		Solve the given expressions with Boolean simplification: i) $C + \overline{(BC)}$ ii) $\overline{AB}(\overline{A} + B)(\overline{B} + B)$	CO1	PO2	**05**
			OR			
2	a)		Implement the given function F = AB + CD using only NAND gates	CO1	PO2	**05**
	b)		Using the Tabulation method and prime implicant table reductions, determine the minimal sum for the Boolean function $f(A,B,C,D)=\Sigma m(1,4,6,7,8,9,10, 11,15)$	CO1	PO2	**10**
	c)		Design a logic circuit for the Boolean function $F(A, B, C, D) = \sum m(0, 1, 2, 5, 8, 9, 10)$ using Product of Sum form.	CO1	PO2	**05**
			UNIT - II			
3	a)		Illustrate a 4-bit carry look ahead adder and mention its advantages over conventional adder circuits.	CO2	PO2	**10**
	b)		Implement the following function $F(abcd)=\sum m(0,1,2,4,6,9,12,14)$ using 4:1 mux considering A & B as select lines.	CO2	PO2	**10**
			OR			
4	a)		Design a single digit BCD adder to add given two decimal numbers.	CO2	PO2	**10**
	b)		Obtain the minterm expression for the following function using a PROM, i) $f_1(A,B,C) = A.B + B'.C$ ii) $f_2(A,B,C) = (A+B'+C).(A'+B)$ iii) $f_3(A,B,C) = A + B.C$	CO2	PO2	**10**

			UNIT - III			
	5	a)	Derive the characteristic equation and excitation table for the following flip flops. i)J K Flip flop ii) T flip flop	*CO2*	*PO2*	**10**
		b)	Justify how the race around condition can be eliminated using Master slave JK flip flop with suitable timing diagram.	*CO2*	*PO2*	**10**
			OR			
	6	a)	Define Shift register. Explain the following operations of shift registers. i) SISO ii) SIPO iii) PIPO iv) PISO	*CO2*	*PO2*	**10**
		b)	Design a MOD-6 asynchronous up counter using JK flip flop. Write the timing diagram for the same.	*CO2*	*PO2*	**10**
			UNIT - IV			
	7	a)	Design a synchronous circuit using positive edge triggered JK flipflop with minimal combinational gating to generate the following sequence. i) 0-1-2-0 if input X=0 ii) 0-2-1-0 if X=1 Provide an output which goes high to indicate the non-zero states in the 0-1-2-0.	*CO3*	*PO3*	**12**
		b)	Differentiate between Mealy and Moore Models.	*CO3*	*PO3*	**08**
			OR			
	8	a)	Design synchronous MOD-6 counter using clocked JK flip flops to sequence 0-2-3-6-5-1	*CO3*	*PO3*	**12**
		b)	Draw the state diagram of a Moore machine to output a "1"if the input has been 1 for three consecutive clock cycles	*CO3*	*PO3*	**08**
			UNIT - V			
	9	a)	With a neat circuit diagram, explain the working of 2 input TTL NAND gate	*CO2*	*PO1*	**10**
		b)	Define the following. i) Fan-in ii) Fan-out iii) Propagation delay iv) Power dissipation	*CO2*	*PO1*	**10**
			OR			
	10	a)	Explain the working of 2 input CMOS NOR gates in detail.	*CO2*	*PO1*	**10**
		b)	Elaborate the characteristics of CMOS and TTL logics and compare the same.	*CO2*	*PO1*	**10**

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