U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

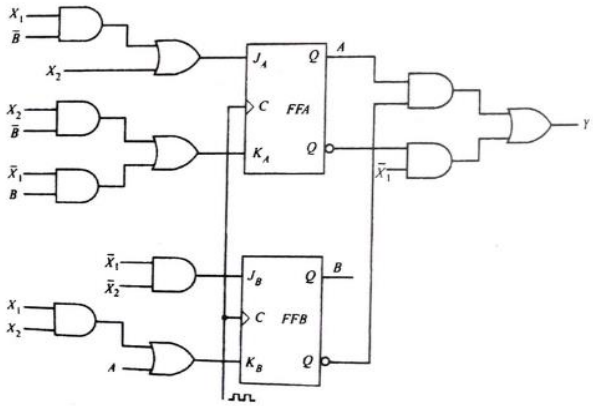
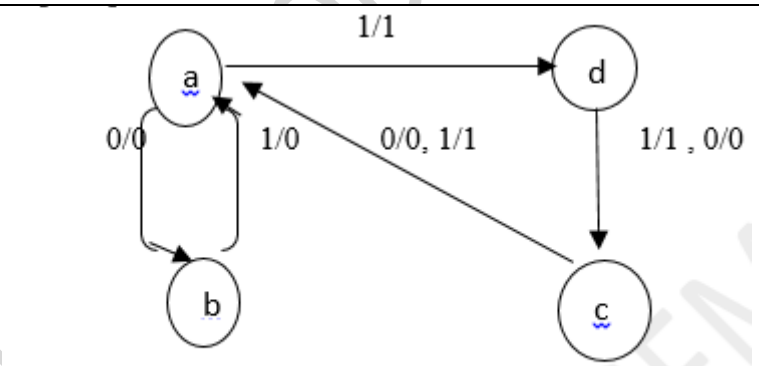
April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: ES Cluster (EEE/ET/EIE/MD) **Duration: 3 hrs.**
Course Code: 23ES3PCDEC **Max Marks: 100**
Course: Digital Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Represent the following functions in minterm and maxterms. i) F= A+BC ii) F= XY+$\bar{X}$ Z	CO1	PO1	**05**
	b)	Find the prime implicants and essential prime implicants for the following function using K-map technique f (A, B, C , D) = ∑m (0,2,5, 7, 8, 10, 13, 15) +dc(1,4,11,14)	CO1	PO1	**07**
	c)	Simplify the following Boolean function by using Quine-McClusky method and determine the prime implicants F (A, B, C , D) = ∑ (1,4,6,7,8,9,10,11,15)	CO1	PO1	**08**
		UNIT - II			
2	a)	Implement the given Boolean function using 4 : 1 multiplexer F (A, B, C) = ∑ (0, 4, 5, 6) .	CO2	PO2	**04**
	b)	Implement the following two Boolean functions with a PLA: F1(A, B, C) = ∑(0, 1, 2, 4) and F2(A, B, C) = ∑(0, 5, 6, 7)	CO2	PO2	**08**
	c)	Explain carry look ahead generation with the help of logic diagram (4-bit).	CO2	PO2	**08**
		OR			
3	a)	Design a 2-bit magnitude comparator to compare two 2 bit number with logic diagram.	CO2	PO2	**10**
	b)	Implement the following Boolean pairs using a decoder with minimum input gates F1(a,b,c)=πM(1,2,4,6) F2(a,b,c)=πM(2,4,7)	CO2	PO2	**04**
	c)	Design a 3-bit binary to gray code converter using a ROM.	CO2	PO2	**06**
		UNIT - III			
4	a)	What is race around condition in flip flops? Explain how it can overcome?	CO2	PO2	**06**
	b)	Convert JK flip flop to D flip flop.	CO3	PO3	**06**

		c)	Design a synchronous Mod-6 (count sequence 0, 1, 2, 3, 4, 5) counter using clocked D flip-flops.	*CO2*	*PO2*	**08**
			OR			
	5	a)	Explain the working of a Master-slave JK flip flop with functional table and timing diagram.	*CO2*	*PO2*	**08**
		b)	Design a 4-bit ripple up counter using negative edge triggered JK flip flops	*CO3*	*PO3*	**05**
		c)	Convert with the help of function table and excitation table JK flip flop to SR flip flop.	*CO2*	*PO2*	**07**
			UNIT - IV			
	6	a)	Construct the excitation table, transition table, state table and state diagram for the synchronous sequential circuit shown in Figure 6.a  Figure 6.a	*CO3*	*PO3*	**12**
		b)	 State Assignment **a :00 b:01, c:10, d:11** Design a sequential circuit for the above state diagram using T-FFs	*CO3*	*PO3*	**08**
			UNIT - V			
	7	a)	Design a CMOS inverter and explain its operation. Compare its characteristics over TTL logic families such as Fan - in, Fan – out, power dissipation, propagation delay, switching speed and noise margin.	*CO1*	*PO1*	**14**
		b)	With circuit schematic explain the working of a two - input TTL NAND gate.	*CO1*	*PO1*	**06**

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