U.S.N.										

B.M.S.College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Semester End Main Examinations

Programme: B.E. **Semester: IV**
Branch: EEE/ECE/EIE/ETE/MD **Duration: 3 hrs.**
Course Code: 22ES4PCAPP **Max Marks: 100**
Course: ARM Processor and Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			CO	PO	Marks
		MODULE - I			
1	a)	With the help of a functional block diagram, explain the essential modules of a computer	*CO1*	*PO1*	**06**
	b)	Analyze the working of memory cell using a neat circuit diagram.	*CO2*	*po2*	**06**
	c)	For the following processor, obtain the performance. Clock rate = 800 MHz .No. of instructions executed = 1000. Average no of steps needed / machine instruction = 20. Also comment on other performance parameters of the processer in general.	*CO2*	*PO2*	**08**
		MODULE - II			
2	a)	What is a Barrel Shifter? Elaborate the working of Barrel Shifter in ARM Data flow model,	*CO2*	*PO2*	**06**
	b)	Indicate the conditional flags updated by ALU operations in ARM processor. With instruction examples illustrate the operation of a Carry Flag and Zero Flag	*CO2*	*PO2*	**06**
	c)	Select a set of memory locations starting from location 'X' to 'X+10'.Assume that a block of date is stored in them. Write the flow chart and the program in Assembly level, to transfer this block of data to another block having the starting address as 'Y' and ending address as 'Y+10'.Justify Looping operation in this program.	*CO2*	*PO2*	**08**
		OR			
3	a)	With example elaborate on the following Assembler Directives. (i)AREA (ii)DCB (iii)ENTRY (iv)DCW	*CO2*	*PO2*	**06**

		b)	With an example for each, differentiate (i)Pre and Post indexing in indirect addressing (ii)Conditional and Unconditional Branch operation (iii)Base and Offset address with Scaling in Indirect addressing	*CO2*	*PO2*	**06**

		c)	Analyze the following code segment and comment on branch operations used in the program.
			CMP r1, r2
			BEQ Complete
			BLT Label1
			SUB r1, r1, r2
			B Label2
			Label1 SUB r2, r2, r1
			B Label2
			Complete NOP
			END
			Label2 MUL r1, r1, r2
			B Complete
				CO2	*PO3*	**08**

			MODULE - III			

	4	a)	Int checksum(int *data)
			{
			char i;
			int sum=0;
			for(i=0;i<;64;i++)
			{
			sum=+ data[i];
			}
			return sum;
			}
			In the above Embedded 'C' code segment, identify the data types and the concept of looping applied
				CO3	*PO3*	**06**

		b)	How do you implement function call using ARM Embedded 'C' program? Illustrate with an example	*CO3*	*PO3*	**07**

		c)	Convert the following code segment to its equivalent assembly level program
			short checksum(short *data)
			unsigned int i;
			int sum = 0;
			for(i=0; i<64; i++)
			{
			sum+= *(data++);
			}
			Return (short)sum;
			}
				CO3	*PO3*	**07**

			OR			
	5	a)	What are 'short' and 'long' data types in ARM Embedded 'C' program? Write an Embedded 'C' program to add five, 16-bit numbers stored from memory location 'x'. Use 'Ç' pointer to read data from memory.	*CO3*	*PO3*	**06**
		b)	How does the register allocation take place in Embedded 'C' program running on ARMTDMI processor? Write a 'C' function to illustrate fixed number of iterations in 'C' looping.	*CO3*	*PO3*	**08**
		c)	What do you mean by instruction scheduling? How is it implemented? Explain.	*CO3*	*PO3*	**06**
			MODULE - IV			
	6	a)	What are subroutines? How do you call subroutines from the main Program? With the help of a program explain calling a subroutine and stack utilization	*CO4*	*PO4*	**08**
		b)	Develop the code to enable and disable IRQ interrupt with appropriate comments.	*CO4*	*PO4*	**05**
		c)	List any three vectored interrupts supported by ARM processor. Explain the sequence of operations to be taken place upon the occurrence of any interrupt.	*CO4*	*PO4*	**07**
			MODULE - V			
	7	a)	With the functional block diagram, elaborate on the working of LPC2148 microcontroller	*CO5*	*PO3*	**07**
		b)	What is a PINESELECT register? Configure the register for different peripheral operations.			**06**
		c)	Explain the fundamental components of an Embedded operating system.			**07**

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