U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

August 2024 Semester End Main Examinations

Programme: B.E. **Semester: IV**
Branch: EEE/ECE/EIE/ETE/MD **Duration: 3 hrs.**
Course Code: 22ES4PCAPP **Max Marks: 100**
Course: ARM Processor and Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed. 3. Internal Choice Units 2&3

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		MODULE - I	CO	PO	Marks
1	a)	Outline the Harvard and Von-Neumann Style of Processor /Controller Architectures with a neat diagram. Analyze the advantage and disadvantage of each architecture	CO2	PO2	**06**
	b)	Explain the operating steps for program execution using a neat diagram showing the connections between processor (identify the different elements of the processor) and memory.	CO1	PO1	**08**
	c)	Identify the advantages and disadvantages of single bus structure and Multiple bus structure	CO1	PO1	**06**
		MODULE - II			
2	a)	Explain ARM core dataflow model with a neat diagram	CO1	PO1	**08**
	b)	Analyze atleast five features of ARM instruction set that make it suitable for embedded applications.	CO2	PO2	**06**
	c)	Develop an ARM Assembly Language Program to find the largest of a number in a series of seven 32 bit numbers stored in memory	CO3	PO3	**06**
		OR			
3	a)	Analyze how the CPSR helps to monitor and control internal operations of the ARM Processor.	CO2	PO2	**06**
	b)	Explain the single register and multiple register Load-Store instructions with examples.	CO1	PO1	**08**
	c)	Analyze the Code snippet for Pre- and Post- values, indicating clearly what the instructions do and provide the Post-values: (i) PRE: R1 = 0x11111111, R2 = 0x01100101 INSTRUCTION : **BIC R0, R1, R2** (ii) PRE: R2 = 0XA0000030, R0 = 0x0000000 INSTRUCTION : **MOV R0, R2, ASR #2**	CO2	PO2	**06**

			(iii) PRE: R0 = 0X00000000, R1 = 0x00000077 INSTRUCTION : **RSB R1, #0**			
			MODULE - III			
	4	a)	Using the checksum function written in C (for N items of integer data), analyze (with corresponding assembly code) how the use of a DO-WHILE loop provides a more efficient implementation than a for-loop using a countdown counter.	*CO2*	*PO2*	**10**
		b)	What is the guidance for efficient use of C-types	*CO2*	*PO2*	**05**
		c)	What do you mean by instruction scheduling? explain	*CO3*	*PO3*	**05**
			OR			
	5	a)	Using the checksum function written in C (for N items of integer data), analyze (with corresponding assembly code) how the use of LOOP UNROLLING provides a more efficient implementation	*CO2*	*PO2*	**08**
		b)	What is the guidance for writing loops effectively	*CO2*	*PO2*	**05**
		c)	List 'c' data types. Explain the disadvantage of using 'char' data type in Embedded C program.	*CO3*	*PO3*	**07**
			MODULE -IV			
	6	a)	Articulate mapping of ARM modes with exceptions and describe the Interrupt Vector table.	*CO4*	*PO4*	**06**
		b)	Outline the steps involved in the structured design of a non-nested interrupt handler routine with a neat diagram	*CO4*	*PO4*	**08**
		c)	Identify the different types of interrupts available with the ARM Processor and briefly explain them.	*CO4*	*PO4*	**06**
			MODULE - V			
	7	a)	Explain the architecture of LPC 2148 and discuss its salient features.	*CO5*	*PO5*	**08**
		b)	Distinguish between the terms 'Firmware' and 'Bootloader'	*CO5*	*PO5*	**06**
		c)	Explain the fundamental Components of an Embedded Operating System	*CO5*	*PO5*	**06**

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