

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February 2025 Semester End Main Examinations

Programme: B.E.

Branch: EEE/ECE/ETE/EIE/MDE

Course Code: 23ES4PCAPP

Course: ARM Processor and Programming

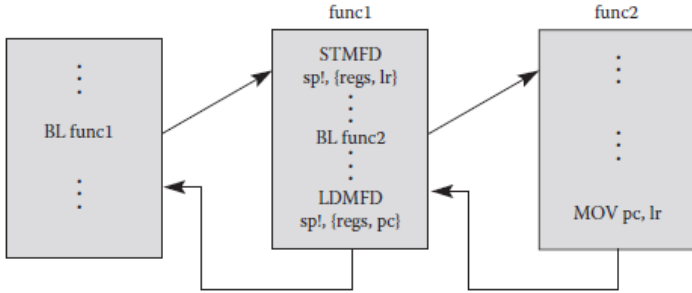
Semester: IV

Duration: 3 hrs.

Max Marks: 100

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.			MODULE - I	CO	PO	Marks
	1	a)	Identify the CISC and RISC features of ARM. Analyze the ARM design philosophy	CO1	PO1	10
		b)	List the registers of ARM processor and explain how are they referred in Load/Store architecture for loading/storing the memory location content in user mode	CO1	PO1	10
			OR			
	2	a)	Explain the control bits of CPSR register. How ALU functioning is reflected in control flag bits? Explain the operation of Zero Flag and Carry flag	CO1	PO1	10
		b)	With an example each, give the applications of ARM processors	CO1	PO1	10
			MODULE - II			
	3	a)	Identify the addressing mode and differentiate operation of the following instructions. i. LDR R1, [R0, #0x4] ii. STR R1, [R0], #0x4	CO2	PO2	04
		b)	Analyze the following instructions and write appropriate addressing mode and output. Given: r0 = 0x00000000, r1 = 0x00080000, mem32[0x00008000] = 0x02020202 mem32[0x00008004] = 0x03030303 a) LDR r0, [r1, #4]! b). LDR r0, [r1, #4] c). LDR r0, [r1], #4 d) STR r0,[r1,#12] , r1=0x200, r0=0x55 e) LDMIA r0!, {r1-r3}	CO2	PO2	06

		MODULE - IV			
7	a)	 <p>The diagram illustrates the execution of two subroutines, func1 and func2. func1 is called from BL.func1. It pushes its return address (BL.func2) onto the stack and then calls func2. func2 pushes its return address (MOV pc, lr) onto the stack and then returns to func1. func1 then returns to BL.func1. The stack grows downwards, with higher addresses at the top and lower addresses at the bottom.</p> <p>Fig.1 Subroutine</p> <p>The Fig.1 shows the stacking the link register during the subroutine execution. Elaborate on the subroutine concept with relevant instructions used and the sequence of operations performed during the execution of subroutines.</p>	CO4	PO2	10
	b)	How are subroutines different from Interrupt service routines? Explain the sequence of operations whenever any of the Exceptions are activated in ARM processor	CO4	PO2	10
		OR			
8	a)	Illustrate the working of IRQ handler in ARM Processor. The illustration must include an example with main program and an IRQ handler, indicating stack utilization.	CO4	PO3	10
	b)	What is stack? How do you access Stack using LDM and STM instructions? Explain Stack Operation in general	CO4	PO3	10
		MODULE - V			
9	a)	Develop a program to configure the DAC module of LPC 2148 for the square waveform generation	CO5	PO3	10
	b)	With the help of register configurations build the program to transmit a string of characters serially using ARM based LPC2148 microcontroller	CO5	PO3	10
		OR			
10	a)	Develop a program to configure the DAC module of LPC 2148 for the triangular waveform generation	CO5	PO3	10
	b)	Write an embedded C program to blink the LEDs connected to P1.24 to P1.31 with appropriate comments	CO5	PO3	10
