U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: IV**

Branch: EEE/ECE/ETE/EIE/MD **Duration: 3 hrs.**

Course Code: 23ES4PCAPP **Max Marks: 100**

Course: ARM Processor & Programming

Instructions: 1.Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Identify the operating modes of ARM architecture and illustrate the banked registers used with operating mode switch.	-	-	**8**
	b)	Differentiate between CISC and RISC computer architectures.	*2*	*2*	**6**
	c)	Analyze the 3-stage pipeline with the following instructions: ADD, SUB and CMP in a sequence. How many cycles are required for the sequence to complete execution?	*2*	*2*	**6**
		OR			
2	a)	Illustrate the data flow model of ARM7TDMI and briefly explain the functional blocks.	-	-	**8**
	b)	Explain the bit specification of Current Program Status Register.	*2*	*2*	**6**
	c)	Compare the features of Von-Neuman and Harvard architectures.	*2*	*2*	**6**
		UNIT - II			
3	a)	Pre Conditions- r0= 0X0000000C, r1= 0X00000018, r2= 0X00000080, Show the corresponding post conditions, after executing each instruction individually i. STRB r0, [r1, - r2, LSR #4]! ii. SUBS r0, r1, r2, LSL #4	*1*	*1*	**10**
	b)	Write an assembly program to find the largest number in an array of 10 words defined in data memory. Use the assembler directives appropriately.	*1*	*1*	**10**
		OR			
4	a)	Identify the addressing mode and differentiate operation of the following instructions. i. LDR R1, [R0, #0x4] ii. STR R1, [R0], #0x4	*1*	*1*	**5**
	b)	With the usage of BX and BLX, analyze how to implement ARM-Thumb interworking.	*2*	*2*	**7**

		c)	Write an assembly program to add five 16-bit data given in an array defined in memory and store back the result in memory.	*1*	*1*	**8**
			UNIT - III			

	5	a)	Write the assembly code for the given 'C' function and analyze its efficiency compared to the assembly of 'for' loop usage.
			int checksum(int *data, unsigned int N)
			{
			int sum=0;
			do
			{
			sum += *(data++);
			} while (--N!=0);
			return sum;
			}
				2	*2*	**10**

		b)	What are the different data types ARM C compiler supports? Briefly discuss on the efficient use of 'C' data types.	*2*	*2*	**10**
			OR			

	6	a)	Given a 'C' function as below; write the compiler assembly code where both the input arguments and return values are type cast.
			short add_v1(short a, short b)
			{
			return a + (b>>1);
			}
				2	*2*	**10**

		b)	Give examples of different instructions sequence and Illustrate various conditions of pipeline stall on ARM9TDMI.	*2*	*2*	**10**
			UNIT - IV			
	7	a)	Show the stack structure and registers updated, with the execution of the following instructions. STMED sp!, {r0-r3} LDMED sp!, {r5-r8} Pre Conditions- r0= 0X0000000C, r1= 0X00000018, r2= 0X00000080, r3=0X00001122 and SP= 0X0000F008	*1*	*1*	**10**
		b)	Explain the steps to be followed by ARM core, while entering and exiting the exception handler.	*2*	*2*	**10**
			OR			
	8	a)	With an example assembly code, explain how to enable and disable IRQ & FIQ exception when the ARM core is in a privileged mode.	*1*	*1*	**10**
		b)	Analyze and justify what address should be retrieved from 'lr' while returning from each of 7 exceptions.	*2*	*2*	**10**

			UNIT - V			
	9	a)	With the architecture diagram of LPC2148, explain the functional blocks in brief.	*2*	*2*	**10**
		b)	Write an embedded C program to blink the LEDs connected to Port-0 pin 24 to pin 31 of LPC2148.	*3*	*3*	**10**
			OR			
	10	a)	What for firmware and bootloader used in embedded system? Briefly discuss on the workflow of firmware.	*2*	*2*	**10**
		b)	Write an Embedded C program to generate a square wave using the DAC port of LPC2148 at P0.16-23 with comments.	*3*	*3*	**10**

******