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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2023 Semester End Main Examinations

Programme: B.E

Branch: ES CLUSTER(EC/EE/ET/EI/ML)

Course Code: 19ES4CCLIC

Course: Linear Integrated Circuits

Semester: IV

Duration: 3 hrs.

Max Marks: 100

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) List FOUR DC- performance characteristics of an OPAMP and explain the same. Also write typical values for 741c IC. **10**

b) AC measuring Instrument need to be designed for finding the peak value of the input waveform, suggest a suitable OPAMP circuit to realize the same. Write its design considerations and explain the working of the same **06**

c) Assuming slew rate of OPAMP is $0.5V/\mu s$, is it possible to amplify a square wave of peak-peak value 50mV with a rise time of $2\mu s$ to a peak-peak amplitude of 1V **04**

OR

2 a) With a suitable OPAMP HF model having a single corner frequency, Obtain the expression for open loop voltage gain. Plot its gain magnitude and phase characteristics. What will be the modification in magnitude plot if the circuit is in closed loop configuration **08**

b) Obtain the expression for gain of an Instrumentation amplifier. Write a suitable block diagram how a Instrumentation amplifier can be used for temperature measurement **08**

c) An inverting amplifier having a flat response up to 40Khz is realized using 741C. The gain of the amplifier is 10. What maximum peak-peak input signal can be applied without distorting the output. **04**

UNIT - II

3 a) Explain a free running oscillator (square wave) with asymmetrical duty ratio using OPAMP. Derive the expression for the period of oscillation. Also write all the relevant waveforms **10**

b) Design an Inverting Schmitt trigger with a UTP = +4V and LTP = +2V. Assume a sinusoidal input signal and $\pm V_{sat} = \pm 10V$. Explain with a circuit, plots and wave forms. Also indicate trigger points . Also plot transfer characteristics **10**

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

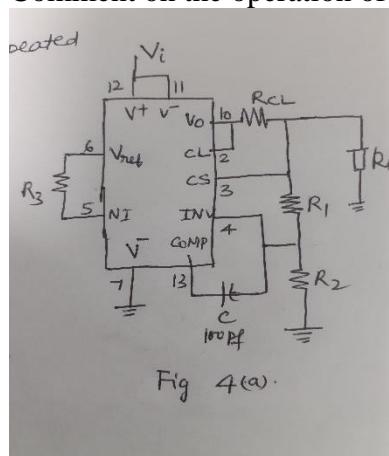
UNIT - III

4 a) Explain current limiting feature in 723 IC. Explain how foldback current limiting in 723, Also compare it with simple current limiting 07

b) With a suitable circuit obtain the expression for gain transfer function $H(j\omega)$ of a 2nd order Butterworth High pass filter with variable gain. Plot its frequency response 07

c) The circuit shown in Fig 4.a is designed for an output voltage of 20V using 723 IC 06

I. Identify the circuit
 II. What is the value of R_{CL} to be used for limiting a maximum current at 0.5A
 III. With R_{CL} connected find output voltage from regulator when $R_L=100\Omega$
 IV. Comment on the operation of the circuit for $R_L=10\Omega$



UNIT - IV

5 a) A 10 bit DAC has a step size of 10mV. Determine the full-scale output and % Resolution 04

b) Explain a SAR type ADC with a suitable block diagram 06

c) A system employs a 16 bit word for representing the input signal. If the maximum output voltage is set to 2V. Calculate the resolution of the system and its dynamic range 04

d) Explain a 2-bit flash type digital to analog converter 06

OR

6 a) An 8-bit ADC accepts an input voltage signal of range 0 to 10V 06

(i) What is the minimum value of the input voltage required to generate a change of 1LSB?
 (ii) What input voltage will generate all 1's at the ADC output?
 (iii) What is the digital output for an input voltage of 4.8V?

b) Explain a sigma delta ADC with the help of a block diagram 06

c) Explain INL and DNL errors for ADC with neat diagrams 04

d) Compare weighted resistor DAC with R-2R ladder DAC 04

UNIT - V

7 a) Explain a ramp generator using 555 timer with suitable waveforms. Write the expression for the period of oscillations and explain the same **06**

b) Design an astable multivibrator using 555 timer for a frequency of 1Khz and a duty cycle of 70%. Assume $C=0.1\mu F$. Write the circuit and indicate the values on the circuit **06**

c) Explain a digital phase detector using suitable waveforms **04**

d) How PLL is used in frequency multiplication/division **04**
