U.S.N.										

B.M.S.College of Engineering, Bengaluru-560019

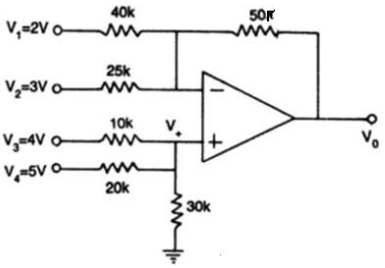
Autonomous Institute Affiliated to VTU

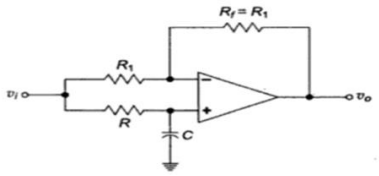
December 2023 Supplementary Examinations

Programme: B.E. **Semester: IV**
Branch: EIE/MD **Duration: 3 hrs.**
Course Code:22ES4PCLIC **Max Marks: 100**
Course: Linear Integrated Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		MODULE - I	CO	PO	Marks
1	a)	Discuss the DC characteristics of op amp 741to be considered with typical values for using in electronic systems.	CO2	PO1	**07**
	b)	Explain the working of a full wave precision rectifier to obtain a positive pulsating output.	CO 2	PO1	**07**
	c)	The input signal V_i to an op amp is 0.04 Sin(1.13×10^5) t, is to be amplified to a maximum extent. How much maximum gain can be obtained by using an op amp with a slew rate of 0.4V/µsec.	CO3	PO2	**06**
		OR			
2	a)	Find V_o for the adder subtractor shown in Fig(1)  Fig(1)	CO3	PO2	**06**
	b)	With a neat circuit diagram, discuss the working of a series op amp regulator.	CO2	PO1	**07**
	c)	Discuss the working of a sample and hold circuit using op amp with neat circuit and waveforms.	CO2	PO1	**07**
		MODULE - II			
3	a)	Describe the working of a Schmitt trigger with neat circuit, equations and waveforms.	CO2	PO1	**07**
	b)	Explain the working of a monostable multivibrator with neat circuit and waveforms. Also derive equation for its pulse width.	CO2	PO1	**08**

		c)	Design a Wien bridge oscillator using op amp to generate a frequency of 2KHz, use C=0.05μf	*CO4*	*PO3*	**05**
			MODULE - III			
	4	a)	Show that $V_o/ V_i = A/ 1+j(f/f_h)$ for a variable gain low pass filter with neat circuit diagram and explain.	*CO3*	*PO2*	**07**
		b)	Design a fourth order low pass Butterworth filter having a cut off frequency of 2kHz. Assume α_1 =0.765, α_2 =1.848 and C=0.1μF.	*CO4*	*PO3*	**07**
		c)	Determine the phase angle and time delay for a circuit shown in Fig(2),for a frequency of 2KHz,assume R_1=20KΩ, R=39KΩ, R_f=R_1, and C=1nF.  Fig(2)	*CO3*	*PO2*	**06**
			MODULE - IV			
	5	a)	Explain the following specification for a DAC i. Monotonicity ii. Resolution	*CO2*	*PO1*	**06**
		b)	Discuss the principle of Successive approximation ADC with a neat circuit diagram.	*CO2*	*PO1*	**08**
		c)	A 12 bit DAC has a step size of 8mV.Determine the full scale output voltage and percentage resolution.Also find the output voltage for an input voltage of (100110011101).	*CO3*	*PO2*	**06**
			OR			
	6	a)	Calculate the value for LSB, MSB and full scale output for an 8 bit DAC for 0 to 10V range.	*CO3*	*PO2*	**06**
		b)	Discuss the working of a weighted resistor DAC with neat circuit diagram, mention its advantages and disadvantages.	*CO2*	*PO1*	**08**
		c)	An 8 bit A to D converter accepts an input voltage of 0 to 10V range (i) What is the minimum value of input voltage required to generate a change of 1 LSB? (ii) What input voltage will generate all 1s at the A to D output? (iii) What is the digital output for 4.8V?	*CO3*	*PO2*	**06**
			MODULE - V			
	7	a)	Explain the Basic principle of working of a PLL with neat schematic diagram.	*CO2*	*PO1*	**08**
		b)	Show that for phase detector used in PLL ,K_{ϕ}= 1.59V /rad, with neat diagram, waveforms and equation.	*CO2*	*PO1*	**06**
		c)	Suggest circuit using PLL for (i) Transmitting binary data by means of two preset carrier frequencies (ii) AM detector	*CO2*	*PO1*	**06**

****