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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science And Engineering **Duration: 3 hrs.**
Course Code: 19IS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture **Date: 13.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may suitably assumed.

UNIT - I

1	a)	With a neat diagram and some simple control commands, list the steps needed to execute the machine instruction Add LOCA,R0 in terms of transfers between the components. Assume that the instruction itself is stored in the memory at location INSTR and this address is initially in register PC.	**08**
	b)	Interpret the different ways of assigning the byte addresses across the words with an example	**04**
	c)	Provide an assembly language program using indexed addressing mode to compute the sum of all scores obtained in each of the tests and store these three sums in memory locations SUM1, SUM2 and SUM3	**08**

UNIT - II

2	a)	Illustrate the program controlled I/O with a program that reads a line from the keyboard, stores it in the memory buffer and echoes it back to the display. Identify the disadvantage of the same.	**06**
	b)	Design an 8-bit parallel port input interface circuit with the significance of its working principles	**08**
	c)	Identify the need for bus arbitration. With a neat diagram explain distributed bus arbitration scheme.	**06**

OR

3	a)	Interpret the timing diagram of an input data transfer using the handshake protocol	**10**
	b)	Define Exception and describe different kinds of exceptions	**10**

UNIT - III

4	a)	Apply Booth's algorithm to multiply the following pair of signed two's complement numbers: A=+23 B= -10 Also implement the above using bit pair recoding algorithm and explain how it acheives faster multiplication.	**10**

	b)	Perform the operation of division using i) restoring and ii) non-restoring method on the following pairs of Numbers: Dividend=11 & Divisor = 3	**10**

UNIT - IV

5	a)	Explain the process of generating control signals for fetching a word from memory operation with suitable diagrams and example.	**10**
	b)	With a neat diagram describe the hardwired control approach for generating the control signals in proper sequence of instruction execution	**10**

OR

6	a)	Write the sequence of control steps required to execute the following operations in a single bus structure: i) Add (R3)+, R1 ii) Add #NUM, R1	**08**
	b)	Interpret the basic organization of MicroProgrammed control unit with a neat diagram	**06**
	c)	Provide the significance of Multibus organization with a neat diagram	**06**

UNIT - V

7	a)	Illustrate the components in a memory hierarchy with a neat diagram	**06**
	b)	Represent and explain the Memory Address Map of RAM and ROM with an assumption that a computer system needs 512 bytes of RAM and 512 bytes of ROM.	**06**
	c)	Explain the hardware organization and instruction execution steps for a 4-stage pipelined processor	**08**

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