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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 22IS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Convert the following pairs of decimal numbers to 5-bit, signed, 2's-complement, binary numbers and add them. State whether or not overflow occurs in each case. **10**

i) 5 and 10 ii) 7 and 13 iii) –14 and 11 iv) –5 and 7 v) –3 and –8

b) List the steps required to execute the machine instruction **Load LOCA, R0** in terms of transfers between the processor components and memory with the following assumptions: **06**

- Instruction itself is stored in the memory at location INSTR which is the initial address of PC.
- To fetch the instruction, update the contents of PC from INSTR to INSTR+1.

c) Register R1 and R2 contain values 1800 and 3800 respectively. The word length of the processor is 4 bytes. What is the effective address of the memory operand in each one of the following cases? **04**

(i) ADD 100 (R2), R6
(ii) LOAD R6, 20 (R1, R2)
(iii) STORE –(R2), R6
(iv) SUBTRACT (R2)+, R6

UNIT - II

2 a) Define Interrupt Service Routine. Explain how an equivalent circuit for an open-drain bus can be used to implement a common interrupt request line for serving N several devices with a neat diagram. **10**

b) Analyze the timing diagram of an input data transfer using the handshake protocol. **10**

OR

3 a) Analyze the solutions for handling the simultaneous arrivals of interrupt requests by the processor from two or more devices that share an interrupt request line. **08**

b) Identify the Bus Arbitration Scheme used when all the devices participates in the arbitration process and explain the same. **06**

c) Outline the significance of registers used in the DMA Controller to carry out the transfer of data block directly between the external device and main memory. **06**

UNIT - III

4 a) Apply Booth's Algorithm to multiply the following pair of signed two's complement numbers: **10**

A=+23
B= -10

Also implement the above using Bit Pair Recoding algorithm and explain how it acheives faster multiplication.

b) Perform the operation of division using a) Restoring and b) Non-Restoring method on the following pairs of numbers: Dividend = 11 and Divisor = 3. **10**

UNIT - IV

5 a) Explain with a neat diagram the process of generating control signals for fetching a word from memory operation with an example. **10**

b) With a neat diagram describe the hardwired control approach for generating the control signals in proper sequence of instruction execution. **06**

c) Explain the hardware organization and instruction execution for a 4-stage pipelined processor with an example. **04**

OR

6 a) Provide the sequence of control steps required to execute the following operation in a single bus structure: **08**

- Add (R3)+, R1

b) Analyze the execution of control sequence of steps for an unconditional branch instruction with an example **08**

c) Define hazards in pipeline concept and outline the types of hazards. **04**

UNIT - V

7 a) Illustrate the components of a memory hierarchy with a neat diagram. **06**

b) Consider a Direct Mapped Cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find- **08**

i) Number of Bits in Block Offset
ii) Number of Bits in Line Number
iii) Number of Bits in Physical Address
iv) Size of Main Memory

c) Paraphrase the direct mapping function with an example. **06**

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