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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 22IS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	List the steps required to execute the given instruction **Add R1,R2,R3** in terms of transfers between the processor and the memory with a neat diagram.	CO2	PO1	**08**
	b)	Generate 5-bit, signed, 2's complement binary representations for the provided pairs of decimal numbers and perform addition. Also, determine whether overflow occurs in each case. i)-39+92 ii)104+45 iii)-1+1 iv)80+80	CO2	PO1	**04**
	c)	Define effective address in addressing modes. Assume register R1 and R2 contain values 1200 and 4600 respectively. The word length of the processor is 4 bytes. What is the effective address of the memory operand in each one of the following cases(Each instruction is independent)? 1) Load 20(R1),R5. 2) Move #3000,R5 3) Store R5,30(R1,R2) 4) Add -(R2),R5 5) Subtract (R1)+,R5	CO2	PO1	**08**
		UNIT - II			
2	a)	Define WMFC and Why is Wait-for-Memory-Function-Completed step needed when reading from or writing to the main memory?	CO1		**04**
	b)	Provide the control sequence for an instruction Add R4, R5, R6 with three bus organization and explain the same.	CO2	PO1	**08**
	c)	Describe the organization of Hardwired control unit with a neat diagram.	CO1		**08**
		OR			
3	a)	Identify the disadvantage of single bus organization and explain the architecture of multiple bus organization with a neat diagram.	CO1		**10**
	b)	Write the sequence of control steps required for the single bus structure in each of the following instructions: I) Add #NUM, R1 ii) Add LOCA, R1	CO2	PO1	**10**

SUPPLEMENTARY EXAMS 2024

			UNIT - III			
	4	a)	Perform multiplication using Booth's algorithm and Bit-Pair Recoding algorithm for the following: i)Multiplicand**:+13** and Multiplier**: -6** ii) Multiplicand**:-11** and Multiplier**: +27**	***CO2***	***PO1***	**08**
		b)	With a neat diagram interpret the design of n-bit adder /subtractor with a example	***CO3***	***PO2***	**06**
		c)	Perform Non-Restoring division for the given binary numbers: Dividend=1010 and Divisor=0011	***CO2***	***PO1***	**06**
			UNIT - IV			
	5	a)	Three devices, A, B, and C, are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases: i. The computer has one interrupt request line. ii. Two interrupt request line, INTR1 and INTR2, are available. INTR1 has higher priority. Specify when and how interrupts are enabled and disabled in each case.	***CO2***	***PO1***	**05**
		b)	Identify and explain the schemes that resolve the issue of simultaneous arrivals of interrupt requests from two or more devices.	***CO1***		**08**
		c)	Interpret the timing diagram for synchronous input data transfer considering propagation delays.	***CO3***	***PO2***	**07**
			OR			
	6	a)	Specify the need for bus arbitration and illustrate the process of distributed arbitration with an example.	***CO3***	***PO2***	**10**
		b)	Design a timing diagram to perform data transfer using handshake protocol during an input operation	***CO3***	***PO2***	**10**
			UNIT - V			
	7	a)	Provide the significance of Memory Hierarchy with a neat diagram w.r.t speed, cost and size	***CO2***	***PO1***	**06**
		b)	Explain the hardware organization and instruction execution for a 4-stage pipelined processor	***CO3***	***PO2***	**06**
		c)	Interpret the Set Associative mapping technique with an example.	***CO1***		**08**

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SUPPLEMENTARY EXAMS 2024