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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 22IS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture **Date: 08.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Given a High-Level language statement C=A+B. Analyze the different basic instruction types which can be used to represent the above statement.	**06**
	b)	Write an Assembly language program to perform Addition of N numbers.	**05**
	c)	Convert the following pairs of decimal number to 4 bits signed 2's complement binary numbers and add them. State whether or not overflow occurs. i) +4 and -6 ii) - 5 and -2	**05**
	d)	Differentiate between Direct and Indirect Addressing modes.	**04**

UNIT - II

2	a)	With a neat diagram, explain the working of interrupt hardware circuit.	**05**
	b)	Device A and Device B sends an interrupt request to the processor simultaneously. Identify and explain the different schemes used by the processor to handle simultaneous interrupts.	**10**
	c)	Identify the technique and the registers used to transfer large blocks of data at high speed between the external device and the main memory.	**05**

OR

3	a)	Interpret the need for Bus Arbitration. Device A with ID 0001 and Device B with ID 0110 sends a request for accessing the bus. Identify the device that gains the bus mastership and explain the same with a diagram.	**10**
	b)	Explain with neat timing diagram, the data transfer during an input operation using Synchronous and Asynchronous Bus.	**10**

UNIT - III

4	a)	Multiply the given pair of signed 2's complement numbers using Booth's Algorithm and verify the answer. Multiplicand X = 110101 Multiplier Y = 011011	**06**

b) Using Sequential circuit binary multiplier, perform multiplication, A=14 and B=7 where A is the multiplicand and B is the multiplier. Infer the circuit design for the same. **08**

c) Given the Dividend X = 17 and Divisor Y = 3, Solve the given problem using Non-Restoring Division. **06**

UNIT - IV

5 a) Provide the control signals generated for the execution of the following instructions with explanation. **10**

i) Add A, R2 where A is the address of the memory location

ii) Sub (R7)+, R6

b) Infer Single Bus Organization of the datapath inside a processor with a neat diagram. **10**

OR

6 a) Write the control sequence for the execution of the instruction Add R4, R5, R6 for a three-bus organization. **05**

b) With a neat diagram, explain Hardwired Control unit organization. **08**

c) Given four stages of a pipelined processor: IF, ID, EX and WB. The IF, ID and WB stages takes one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD instruction needs 2 clock cycles, SUB instructions needs 3 clock cycles and the MUL instruction needs 4 clock cycles in the EX stage. **07**

Represent with a diagram the number of clock cycles taken to complete the following sequence of instructions and highlight advantage of using pipelining.

ADD A, R4
SUB (R5)+, R6
MUL –(R1), R2

UNIT - V

7 a) Design a Memory of 2M x 32 using 512K x 8 static memory chips. Analyze the number of chips and the address lines needed to design the above memory. **10**

b) Design Direct Mapping and Associative mapping functions, given a cache consisting of 128 blocks of 16 words each and memory with 4K blocks of 16 words each. **10**

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