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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 23IS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Mention the special purpose registers inside the CPU. With a neat diagram, discuss how CPU and memory interact in executing an instruction.	*CO1*		**10**
	b)	Register R1 and R2 of computer contain the decimal value 1650 and 2400 respectively. What is the effective address of the source operand in each of the following instructions? (Assume 32-bit word length) (i) Load 20(R1), R2 (ii) Move #3050, R5 (iii) Store 30(R1, R2), R5 (iv) Add –(R2), R5 (v) Subtract (R1)+, R5	*CO2*	*PO1*	**05**
	c)	Convert the following pair of decimal number to 5 bit signed 2's complement binary number and perform addition. State whether overflow occurs or not in each case. i) −10 and +3 ii) −14 and −12	*CO2*	*PO1*	**05**
		UNIT - II			
2	a)	Detail out the internal organization of the processor with single bus for datapath. Represent with a block diagram.	*CO1*		**10**
	b)	Write complete control sequence for execution of the following instructions using single bus organization. i) Add (R3), R1 ii) Unconditional Branch instruction	*CO3*	*PO2*	**10**
		OR			
3	a)	With neat diagram, illustrate three bus organization and write control sequence for the instruction Add R4, R5, R6	*CO3*	*PO2*	**10**

		b)	Interpret the process of generating control signals by control unit through Hardwired approach with a neat diagram.	*CO1*		**10**
			UNIT - III			
	4	a)	Perform multiplication for the given signed numbers using Booth's algorithm and Fast-Bit pair recoding method: i) Multiplicand: +13 and Multiplier: -6 ii) Multiplicand: -11 and Multiplier: +27	*CO2*	*PO1*	**10**
		b)	Write the steps of restoring division algorithm in computer arithmetic. Perform 8 ÷ 3 using restoring division.	*CO2*	*PO1*	**10**
			UNIT - IV			
	5	a)	Device A and Device B sends an interrupt request to the processor simultaneously. Identify and explain the different schemes used by the processor to handle simultaneous interrupts.	*CO1*		**10**
		b)	Analyse the timing diagram to perform the data transfer during an input operation using synchronous bus.	*CO3*	*PO2*	**06**
		c)	Specify how exceptions are used in the case of debuggers.	*CO1*		**04**
			OR			
	6	a)	Detail out the types of Bus arbitration with suitable illustrations.	*CO2*	*PO1*	**10**
		b)	Design a timing diagram to perform data transfer using handshake protocol during an input operation.	*CO3*	*PO2*	**10**
			UNIT - V			
	7	a)	Define hazards in pipelining. With a neat diagram, Illustrate the working of a structural hazard with an example.	*CO2*	*PO1*	**10**
		b)	Interpret direct and associative mapping functions relevant to cache memories with appropriate illustrations.	*CO2*	*PO1*	**10**

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