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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## June 2025 Semester End Main Examinations

**Programme: B.E.** **Semester: III**

**Branch: Information Science and Engineering** **Duration: 3 hrs.**

**Course Code: 23IS3PCCOA / 22IS3PCCOA** **Max Marks: 100**

**Course: Computer Organization and Architecture**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

| | | UNIT - I | CO | PO | Marks |
|---|---|---|---|---|---|
| 1 | a) | With a neat diagram, illustrate how CPU and memory interact in executing an instruction by mentioning the purpose of each special purpose registers involved. | CO1 | | 8 |
| | b) | With an example, explain any four addressing modes. Provide an assembly language program to add n numbers with the use of indirect addressing mode. | CO2 | PO1 | 8 |
| | c) | Convert the following pair of decimal number to 5 bit signed 2's complement binary number and perform addition. State whether overflow occurs or not in each case.<br>i) −10 and +3 ii) +14 and −12 iii) +13 and +11<br>iv) − 9 and +14 | CO2 | PO1 | 4 |
| | | **OR** | | | |
| 2 | a) | State and explain the performance equation? | CO1 | | 5 |
| | b) | Sketch the internal organization of CPU out with its functionalities and block diagram. | CO1 | | 5 |
| | c) | Registers R1 and R2 of a computer contain the decimal values 1300 and 5600. Identify the type of addressing modes and find the effective address of the memory operand in each of the following instructions?<br>(a) Load 30(R1),R5<br>(b) Move #4000,R5<br>(c) Store R5,20(R1,R2)<br>(d) Add −(R2),R5<br>(e) Subtract (R1)+,R5 | CO2 | PO1 | 10 |
| | | **UNIT - II** | | | |
| 3 | a) | With a neat diagram, illustrate the working of generating the control sequence using hardwired approach. | CO1 | | 10 |
| | b) | Write complete control sequence for execution of the following instructions using single bus organization.<br>ADD(R3)+,R1 ii) ADD#NUM,R1 | CO3 | PO2 | 10 |
| | | **OR** | | | |

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|---|---|---|---|---|---|---|
| | 4 | a) | With neat diagram, illustrate three bus organization and write a control sequence for the instruction ADD R4,R5,R6. | *CO3* | *PO2* | **10** |
| | | b) | Interpret the steps involved in Fetching a Word from Memory with a neat diagram. | *CO2* | *PO1* | **10** |
| | | | **UNIT - III** | | | |
| | 5 | a) | Perform multiplication for the given signed numbers using Booth's algorithm and Fast-Bit pair recoding method:<br>• Multiplicand: −11 and Multiplier: +27<br>Also explain why bit pair recoding algorithm achieves faster multiplication. | *CO2* | *PO1* | **10** |
| | | b) | Perform restoring division algorithm for the dividend 7 and the divisor 3 with steps. | *CO2* | *PO1* | **10** |
| | | | **OR** | | | |
| | 6 | a) | With a neat diagram, explain the working of a sequential circuit binary multiplier. Perform (−13) x (+11) using sequential multiplication. | *CO2* | *PO1* | **10** |
| | | b) | Design a Combinatorial Array Multiplier for 4 X 4 (No of bits for multiplicand and multiplier=4) | *CO2* | *PO1* | **10** |
| | | | **UNIT - IV** | | | |
| | 7 | a) | Define an interrupt? Illustrate about simultaneous request handling by the processor with a neat sketch | *CO3* | *PO2* | **10** |
| | | b) | Illustrate the program controlled I/O with a program that reads a line from the keyboard, stores it in the memory buffer and echoes it back to the display. Identify the disadvantage of the same | *CO2* | *PO1* | **10** |
| | | | **OR** | | | |
| | 8 | a) | What is DMA? Draw the block diagram for DMA controller and explain about DMA transfer in a computer | *CO1* | | **10** |
| | | b) | Illustrate with a neat diagram, the two approaches of bus arbitration with a neat diagram. | *CO2* | *PO1* | **10** |
| | | | **UNIT - V** | | | |
| | 9 | a) | Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-<br>i) Number of bits in tag<br>ii) Tag directory size | *CO3* | *PO2* | **10** |
| | | b) | Define Hazards and its types. | *CO1* | | **4** |
| | | c) | Illustrate the associative mapping technique with its advantages and disadvantages. | *CO2* | *PO1* | **6** |
| | | | **OR** | | | |
| | 10 | a) | Draw the neat sketch of memory hierarchy and explain the need of cache memory? | *CO1* | | **6** |
| | | b) | Interpret the hardware organization and instruction execution steps for a 4-stage pipelined processor | *CO2* | *PO1* | **6** |
| | | c) | Explain about direct and set associative map technique in cache. | *C02* | *PO1* | **8** |

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