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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Information Science and Engineering **Duration: 3 hrs.**

Course Code: 23IS3PCCOA /22IS3PCCOA /19IS3PCCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	CO	PO	Marks
1	a)	Explain byte addressability and its types with examples.	CO 1		10
	b)	Mention the special purpose registers inside the CPU. With a neat diagram, discuss how CPU and memory interact in executing an instruction.	CO 1		10
		OR			
2	a)	Explain the different addressing modes with an example	CO 1		10
	b)	Provide an assembly language program using indexed addressing mode to compute the sum of all scores obtained in each of the tests and store these three sums in memory locations SUM1, SUM2 and SUM3	CO2	PO1	06
	c)	State the basic performance equation. Explain the significance of each parameter of the equation.	CO2	PO1	04
		UNIT - II			
3	a)	Illustrate the hardwired control approach for generating the control signals in proper sequence of instruction execution with a necessary diagram.	CO2	PO1	10
	b)	Write the sequence of control steps required to execute the following operations in a single bus structure. i) ADD (R3)+,R1 ii) ADD #Num,R1	CO3	PO2	10
		OR			
4	a)	Interpret the generation of control signals for fetching a word from memory and storing a word into memory	CO2	PO1	10
	b)	Analyse how control signals are generated for managing branch instructions. Provide a control sequence steps for the unconditional branch instruction Add(R3), R1.	CO3	PO2	10

			UNIT - III			
	5	a)	Perform restoring division for 10÷3 by representing the algorithmic steps.	***CO3***	***PO2***	**10**
		b)	Determine the constraints of the array multiplier. Illustrate the sequential binary multiplier circuit for unsigned numbers with a neat diagram.	***CO3***	***PO2***	**10**
			OR			
	6	a)	Find the Quotient and Remainder of 25 ÷ 15 using nonrestoring division steps.	***CO3***	***PO2***	**10**
		b)	Sketch and explain the logic circuit that perform addition/subtraction of two 'n' bit numbers X and Y	***CO3***	***PO2***	**05**
		c)	Perform multiplication using Booth's algorithm and Bit-Pair Recoding algorithm for the following: i) Multiplicand: +23 and Multiplier: -10	***CO2***	***PO1***	**05**
			UNIT - IV			
	7	a)	Outline the significance of Bus arbitration and describe the Centralized bus arbitration process with a neat diagram.	***CO2***	***PO1***	**10**
		b)	Interpret the different ways of enabling and disabling interrupts.	***CO3***	***PO2***	**10**
			OR			
	8	a)	Define Asynchronous bus operation. Illustrate the handshake control of data transfer during input operation with the detailed timing diagram.	***CO3***	***PO2***	**10**
		b)	Provide a working of an equivalent circuit of an open drain with a common interrupt request line for handling the request of several I/O devices	***CO3***	***PO2***	**10**
			UNIT - V			
	9	a)	Illustrate pipelining and traditional pipelining concept. Exhibit the hardware organization and instruction execution steps for a 4-stage pipelined processor	***CO2***	***PO1***	**10**
		b)	Describe the different mapping functions relevant to cache memories	***CO2***	***PO1***	**10**
			OR			
	10	a)	Illustrate the components in a memory hierarchy w.r.t speed, size and cost with a neat diagram.	***CO1***		**05**
		b)	Identify the importance of locality of reference and its types in cache memories.	***CO2***	***PO1***	**05**
		b)	A block set associative cache consists of a total of 64 blocks divided into 4 block sets. The MM contains 4096 blocks each containing 128 words. a) How many bits are there in MM address? b) How many bits are there in each of the TAG, SET & word field	***CO3***	***PO2***	**10**

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