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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 23IS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)	List the steps required to execute the given instruction ADD LOCA, LOCB in terms of transfers between the processor and the memory with a neat diagram.		*CO2*	*PO1*	**10**
	b)	Generate 5-bit, signed, 2's complement binary representations for the provided pairs of decimal numbers and perform addition. Also, determine whether overflow occurs in each case. i) -4 and +4 ii)+7 and +7 iii) -6 and -4 iv)-3 and -5 v)+5 and +4		*CO2*	*PO1*	**05**
	c)	Write an assembly language program that can evaluate expression Y=(A-B)/(C+D x E) using two-address and one-address instruction type.		*CO2*	*PO1*	**05**
		UNIT - II				
2	a)	With a neat diagram interpret the process of control signals generation to fetch a word from memory for the register Memory Data Register.		*CO1*		**07**
	b)	Provide the control sequence for an instruction Add R4, R5, R6 with three bus organization and explain the same.		*CO2*	*PO1*	**06**
	c)	Summarize the generation of control signals by control unit through hardwired control approach with a detailed diagram.		*CO1*		**07**
		OR				
3	a)	Identify the advantage of multiple bus organization over the single bus organization and explain the architecture of multiple bus organization with a neat diagram.		*CO1*		**07**
	b)	Write the sequence of control steps required for the single bus structure in each of the following instructions: a) Add the immediate number NUM to register R1. b) Add the contents of memory location NUM to register R1.		*CO2*	*PO1*	**08**
	c)	Provide an example of control sequence steps for a unconditional branch instruction.		*CO2*	*PO1*	**05**

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			UNIT - III			
	4	a)	Perform multiplication using Booth's algorithm and Bit-Pair Recoding algorithm for the following: i)Multiplicand**:+23** and Multiplier**: -10** ii) Multiplicand**:+15** and Multiplier**: +15**	*CO2*	*PO1*	**08**
		b)	Analyse the sequential binary multiplier circuit for unsigned numbers with a neat diagram	*CO3*	*PO2*	**06**
		c)	Solve 25 ÷ 15 using non-restoring division algorithm	*CO2*	*PO1*	**06**
			UNIT - IV			
	5	a)	Specify, how interrupts are useful for the given scenario below: Consider a task that requires some computations to be performed and the results to be printed on a line printer. The program consists of two routines COMPUTE and PRINT. Assume that COMPUTE produces a set of n lines of output, that is to be printed by the PRINT routine.	*CO2*	*PO1*	**06**
		b)	Provide the solution by considering priority and daisy chain schemes, to resolve the issue of simultaneous arrivals of interrupt requests	*CO1*		**08**
		c)	Interpret the timing diagram for synchronous bus to perform input data transfer with propagation delays.	*CO3*	*PO2*	**06**
			OR			
	6	a)	Describe the Distributed Arbitration process in the selection of the next bus master. With Distributed Arbitration process identify the device that gains the bus mastership for the following with a neat diagram: Consider two devices A and B having ID's as 5 and 6, respectively are requesting the use of bus. The pattern that appears on arbitration lines is 0111.	*CO3*	*PO2*	**08**
		b)	Design a timing diagram to perform data transfer using handshake protocol during an input operation	*CO3*	*PO2*	**08**
		c)	Specify how exceptions are used in the case of debuggers	*CO1*		**04**
			UNIT - V			
	7	a)	Provide the mapping technique that is a combination of direct and associative mapping techniques. Clarify the same with an example.	*CO2*	*PO1*	**08**
		b)	Illustrate structural hazard with an example. Suggest a solution to avoid structural hazard in a pipelining concept.	*CO3*	*PO2*	**07**
		c)	Define Locality of reference property and its types with reference to cache mechanism.	*CO1*		**05**

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