U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 19IS3PCDLD **Max Marks: 100**
Course: DIGITAL LOGIC DESIGN **Date: 22.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
Revealing of identification, appeal to evaluator will be treated as malpractice.

SUPPLEMENTARY EXAMS 2023

UNIT - I

1 a) Design a combinational logic circuit to output the 2's complement of a 4-bit binary number. **06**
   i) Construct the truth-table
   ii) Simplify each output function using K-map and write reduced equations
   iii) Draw the resulting logic diagram.

b) Simplify the following Boolean function by using Quine-McCluskey method **08**
F (A, B, C, D) = ∑m (0,2,3,6,7,8,10,12,13)

c) Simplify using K-Map. Write the Boolean equation and realize using NAND gates. **06**
F (W, X, Y, Z) = ∑m (0,2,4,6,8) +∑d (10,11,12,13,14,15)

UNIT - II

2 a) Implement the following Boolean function with an 8:1 MUX with a, b and d connected to selection lines S2, S1, S0 respectively **05**
F (A, B, C, D) = ∑m (0,1,3,4,8,9,15)

b) Design a 2-bit comparator along with the truth-table and logic diagram **05**

c) Implement the following functions using 3X4X2 PLA. **06**
f1(a, b,c)= ∑m(1,2,3,7) f2(a,b,c)= ∑m(1,5,7)

d) Implement the given function using a 3-to-8-line decoder. Minimize the total number of input terminals **04**
$f1(x_2, x_1, x_0) = \sum m (0,1,5,6,7)$ $f2(x_2, x_1, x_0) = \sum m (1,5,7)$

UNIT - III

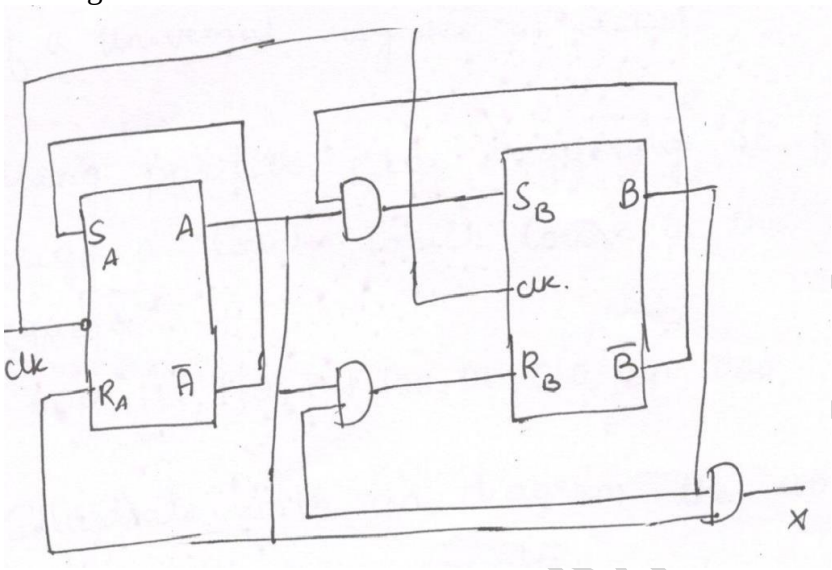
3 a) Along with the truth-table and logic diagram, explain the working principle of **08**
   i) Clocked SR Flip-Flop ii) Clocked JK Flip-Flop iii) Clocked D Flip-Flop

b) Derive the characteristic equations for **12**
i) SR Flip-Flop ii) JK Flip-Flop iii) D Flip-Flop iv) T Flip-Flop

OR

4 a) Design a master-slave JK flip-flop. Draw the logic diagram and explain its working along with truth-table. **10**

b) Analyze the given sequential circuit along with state synthesis table and state transition Diagram. **10**



UNIT - IV

5 a) With a neat diagram, explain the working of a universal shift register. **10**

b) Using positive edge triggered SR flip-flops, design a counter which counts in the following sequence **10**

000,111,110,101,100,011,010,001,000

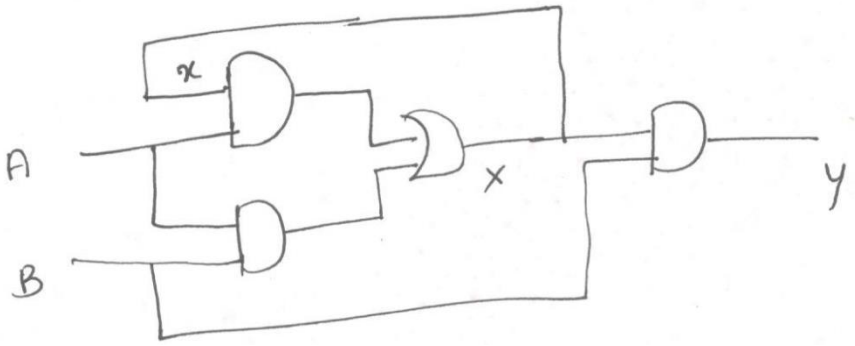
UNIT - V

6 a) Reduce the number of states in the following state table and tabulate the reduced state table using row elimination method. **08**

Present State	Next state		Output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

b) Analyze the mealy model asynchronous sequential circuit of the given figure and show its stable state and corresponding outputs. Give the state diagram of this circuit. **06**

SUPPLEMENTARY EXAM

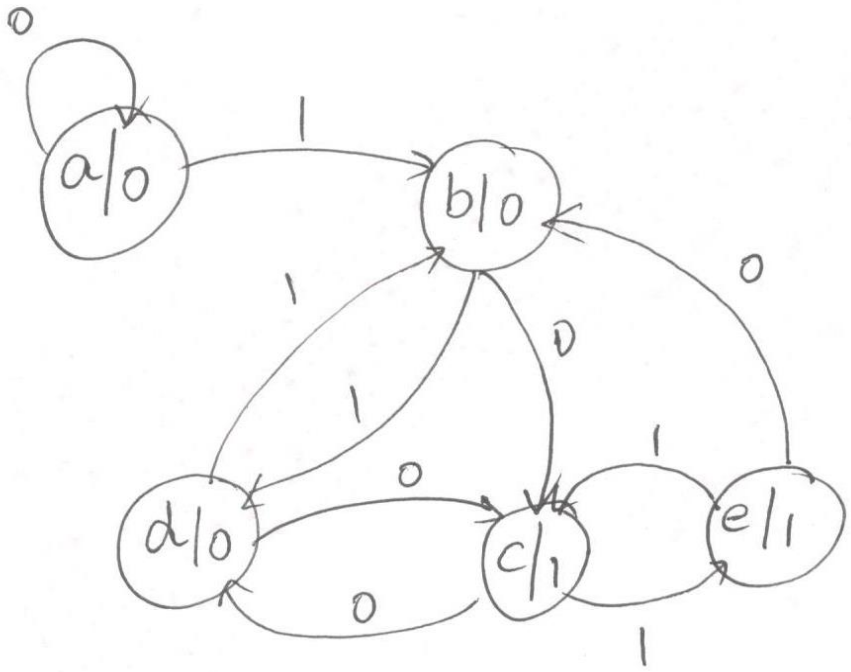


c) Discuss the steps for conversion between Mealy and Moore model. **06**

OR

7 a) Design a Moore model to detect the sequence that receives binary data stream at its input X and signals when a combination '011' arrives at the input by making its output, Y high which otherwise remains low. Consider, data is coming from left i.e. the first bit to be identified is 1, second 1 and third 0 from the input sequence. **10**

b) Reduce the state transition diagram using **10**
i) Row elimination Method ii) Implication table method.



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