U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 22IS3PCDLD **Max Marks: 100**
Course: Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Design a three-input, one-output minimal two-level gate combinational network that has a logic-1 output when the majority of its inputs are logic-1 and has a logic-0 output when the majority of its inputs are logic-0. **06**

b) Express each of the following functions by a minterm canonical formula. **06**
(i) $f(x,y,z) = \bar{x}\,(\bar{y}+z)+\bar{z}$
(ii) $f(x,y,z) = (x+\bar{y})+(x+z)$

c) Design an odd parity generator for a combinational network. The inputs to the network are binary numbers 0 to 15 and output of the network is to produce the corresponding parity bit using an odd parity scheme. **08**

OR

2 a) Using K-map, simplify the following Boolean functions. Obtain minimal sum expressions. **10**
(i) $f(w,x,y,z) = \sum m(0,1,2,5,8,15) + dc(6,7,10)$
(ii) $f(w,x,y,z) = \sum m(2,8,9,10,12,13) + dc(7,11)$

b) Using Quine-McCluskey method, obtain all the prime implicants for the following Boolean function: $f(w,x,y,z) = \sum m(7,9,12,13,14,15) + dc(4,11)$ **10**

UNIT - II

3 a) Explain the organization of a single decade BCD adder. Design the circuit with Correction logic. **10**

b) Realize the function $f(x,y,z) = \sum m(0,2,3,5)$ using **10**
(i) 8:1 line multiplexer with select bits S_2, S_1, S_0 as x, y, z.
(ii) 4:1 line multiplexer with select bits S_1, S_0 as x, y.

UNIT - III

4 a) Design a positive Edge triggered JK flipflop and explain its working with relevant details. **10**

b) Explicate the design of a clocked RS flipflop. **10**

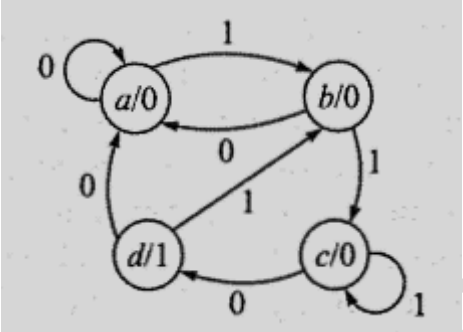
UNIT - IV

5 a) Explicate on the operations performed by Universal Shift Register. Provide details on its design with logic diagram and truth table. **10**

b) Design a Synchronous mod-6 counter using JK flipflops that counts 0 -> 2 -> 3 -> 6 -> 5 -> 1 -> 0. **10**

UNIT - V

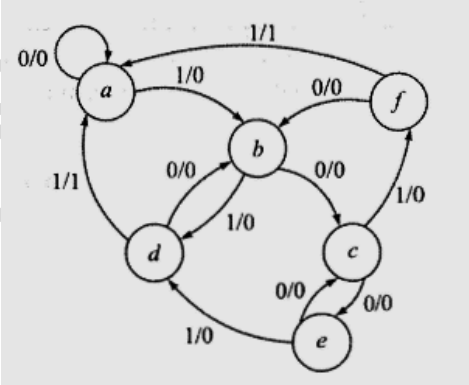
6 a) Design a circuit diagram using Moore model whose transition diagram is given below. Use negative edge triggered SR flipflops. **10**



b) Discuss the problems encountered with Asynchronous sequential circuits using relevant illustrations. **10**

OR

7 a) Consider the following State transition diagram. Identify and remove redundant states to obtain the reduced state diagram using Row Elimination method. **10**



b) Analyze the asynchronous sequential circuit considering **10**
(i) Two input AND gate with output feedback.
(ii) Two input NAND gate with output feedback.

******