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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

August 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 22IS3PCDLD **Max Marks: 100**
Course: Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1	a)	Write each of the following minterm canonical formula in algebraic form and construct their corresponding truth-tables F(w,x,y,z) = ∑m(1,3,7,8,9,14,15)	**05**
	b)	Apply the expansion theorem to the Boolean expressions $f(w,x,y,z) = W'XYZ' + Z(XY' + WX')$	**05**
	c)	Simplify the following Boolean function f(w,x,y,z) =∑m(2,6,8,9,10,11,14,15) using Quine-McCluskey method. Find Prime-implicants and Essential prime-implicants.	**10**

OR

2	a)	Simplify the following Boolean function using K-map F(p,q,r,s)= ∑m(0,2,5,7,9,11) +∑d(3,8,10,12,14)	**05**
	b)	Simplify the following Boolean function using Quine-McCluskey method to find the prime implicants. F(a,b,c,d) = ∑m(7,9,12,13,14,15) +∑dc(4,11)	**10**
	c)	Using universal gates, design a SOP logic circuit for a 3-variable input where the output is high whenever the inputs are 010,100 and 110.	**05**

UNIT - II

3	a)	Realize each of the following Boolean expression using 8:1 MUX where x,y,z appear on Select lines S_2, S1 and S_0 F(w,x,y,z) =∑m(0,4,6,8,9,11,13,14)	**06**
	b)	Implement the following functions using 3X4X2 PLA. F1(a,b,c) =∑m(0,1,3,4) f2=∑m(1,2,3,4,5)	**08**
	c)	Illustrate the working of a 1-bit magnitude comparator with a logic circuit and a relevant truth-table. Simplify using K-maps for the circuit diagram.	**06**

UNIT - III

4	a)	Find the characteristic equation of i) SR Flip-flop ii) JK Flip-flop	**06**
	b)	Illustrate the working of a positive edge triggered D-Flip-flop with a suitable logic circuit diagram and its function table.	**08**

c) Explain the working of RS Flip-flop with a block diagram and functional table. **06**

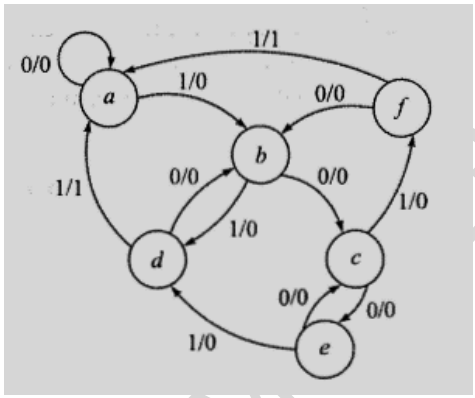
UNIT - IV

5 a) With a neat diagram, explain the working of a Universal Shift Register in detail. **10**

b) Design a 3-bit Synchronous Up-counter using JK Flip-flops. **10**

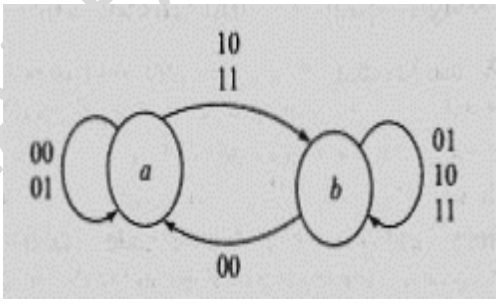
UNIT - V

6 a) Reduce the state transition diagram given below using Row Elimination Method. **07**



b) Differentiate between Moore model and mealy model of Sequential logic circuits. **07**

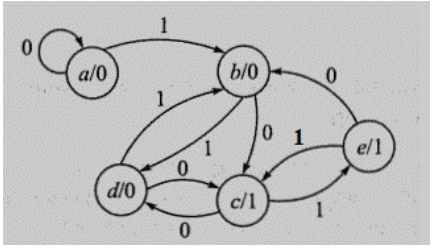
c) Design an asynchronous sequential logic circuit for the following state transition diagram. **06**



OR

7 a) Design a mealy model for detecting the binary data stream 110 with the help of a State Transition diagram, State Synthesis table, Design equations and circuit diagram. **10**

b) Reduce the state transition diagram given below using Row Elimination method. **10**



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