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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 22IS3PCDLD **Max Marks: 100**
Course: Digital Logic Design **Date: 19.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) A four-bit binary number is represented as $A_3A_2A_1A_0$, where $A_3A_2A_1A_0$ represent the individual bits and A_0 is equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000. **10**

b) Using Quine-McCluskey Method, Obtain all the prime implicants for the following boolean function. **10**
f(A, B, C, D) = ∑m (0,2,3,6,7,8,10,12,13)

OR

2 a) Write each of the following minterm canonical formula in algebraic form and construct their corresponding truth tables. **06**
i. f(A, B, C, D) = ∑m (0,2,4,5,7)
ii. f(A, B, C, D) = ∑m (1,3,7,8,9,14,15)

b) Using Boolean algebra postulates and theorms, Simplify each of the following expressions as disjunctive normal formulas with fewest number of literals. **06**
i. $\bar{w}\bar{x}\bar{y}z + w\bar{x}\bar{y}z + xz + xy\bar{z}$
ii. $\bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + x\bar{y}z + xy\bar{z}$

c) Using karnaugh maps, determine all the minimal sums for the following Boolean function: **04**
F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)

d) Given F = ∑m(0, 1, 5, 7, 15, 14, 10), find number of implicants(I), Prime Impicants(PI), Essential Prime Implicants(EPI) and Redundant Prime Implicants(RPI). **04**

UNIT - II

3 a) Realize the following Boolean expression using **10**

$f(w, x, y, z) = \sum m (1,2,6,7,9,11,12,14,15)$

i. an 8-to-1 line multiplexer where x, y and z appear on select lines S_2, S_1 and S_0 respectively.

ii. An 8-to-1 line multiplexer where w, x and y appear on select lines S_2, S_1 and S_0 respectively.

b) Design a 3-to-8 decoder using two 2-to-4 decoders. **05**

c) Implement the following functions using PAL. **05**

$X(A,B,C) = \sum m (2,3,5,7)$
$Y(A,B,C) = \sum m (0,1,5)$
$Z(A,B,C) = \sum m (0,2,3,5)$

UNIT - III

4 a) Differentiate between combinational circuits and sequential circuits. **05**

b) Draw the logic diagram of SR flip flop and explain its working with truth table. **10**

c) Explain the operation of cross coupled NAND gates. **05**

UNIT - IV

5 a) Using Negative edge-triggered D flip flops and waveforms, explain the working of 4-bit SIPO shift register. **10**

b) Design a synchronous counter to count the sequence 0 -> 1 -> 4 -> 6->7 -> 5 -> 0 using positive edge triggered JK flipflops. **10**

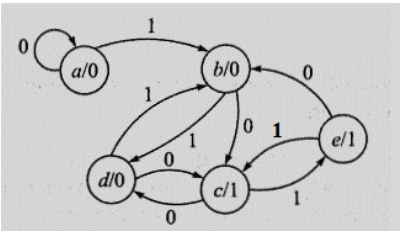
UNIT - V

6 a) Design a Mealy Machine that outputs a 1 whenever the sequence 1010 is encountered in any input binary string. **10**

b) Reduce the below state transition diagram using **10**

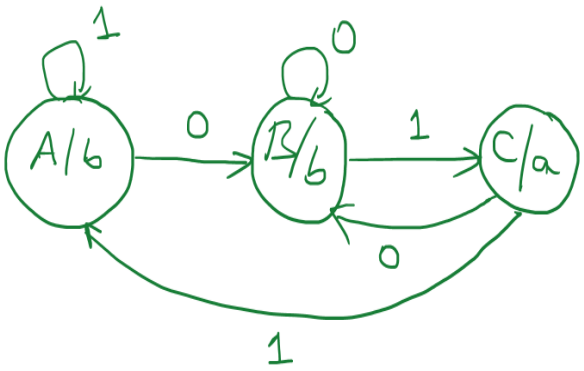
i. Row elimination method

ii. Implication table method

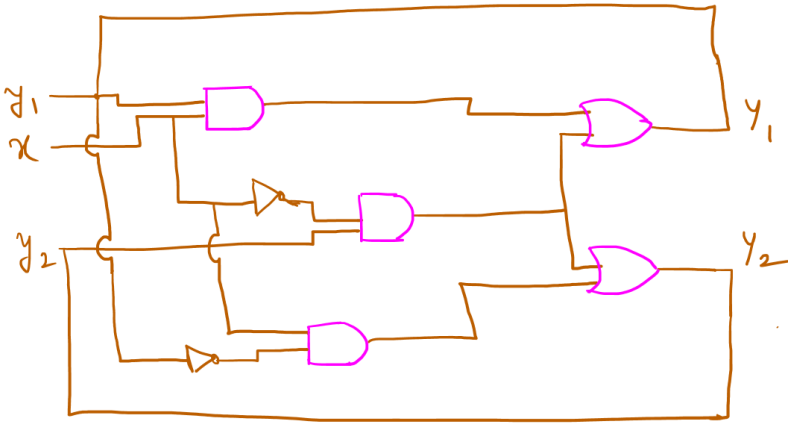


OR

7 a) Elucidate the steps to convert a Mealy machine to Moore machine. Apply the steps to convert the following state transition diagram from Moore model to Mealy model. **10**



b) Analyse the following asynchronous sequential circuit and draw transition maps and state table. **10**



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