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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

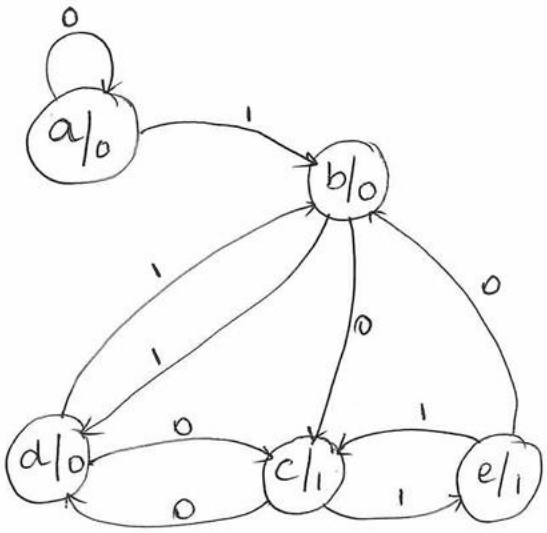
April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 23IS3PCDLD **Max Marks: 100**
Course: Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		State and Prove De-Morgan's theorems.	*CO1*	-	**05**
	b)		Using Karnaugh maps, determine all the minimal sums and minimal products for the following Boolean Functions. i) f(a,b,c,d)= πM(1,5,6,7,9,11,12,13) + dc(0,3,4)	*CO1*	-	**05**
	c)		A Digital system is to be designed in which the months of the year is given as input in 4-bit form. The month January is represented as 0000, February as 0001 and so on. Output of the system should be '1' corresponding to the inputs of the month containing 31 days or otherwise it is '0'. For this system of 4 variables (A, B, C and D) Find the following: i. Boolean expression in ∑m and ϖM form. ii. Write the truth table. iii. Using K-map, simplify the Boolean expression for minterms canonical form. iv. Implement the simplified expression using NAND-NAND gates.	*CO2*	*P01*	**10**
			OR			
2	a)		Using K-map, determine all the minimal sums for each of the following Boolean functions. i. F (A, B, C, D) = ∑m (0,2,4,6,8,9,10,12,14) + d (1,5,11,13) ii. F (W, X, Y, Z) = W'X'Z + XYZ + WX'Z + XY'Z'	*CO2*	*P01*	**10**
	b)		Obtain all the Essential Prime Implicants using Quine-McCluskey method. Realize the simplified expression using NAND gates only. F (A, B, C, D) = ∑m (0,1,2,3,10,11,12,13,14,15)	*CO2*	*P01*	**10**
			UNIT - II			
3	a)		Show the organization of a single decade BCD adder. Design the circuit with correction logic.	*CO2*	*P01*	**10**

		b)	Design a 2-bit magnitude comparator along with the truth-table and logic diagram.	*CO2*	*P01*	**05**
		c)	Implement the following Boolean function with an 8:1 MUX with A, B and C connected to the selection lines S2, S1 and S0 respectively. F (A, B, C, D) = ∑m (0, 1, 3, 4, 5, 7, 9, 13, 15)	*CO2*	*P01*	**05**
			UNIT - III			
	4	a)	With a neat diagram show the operation of JK Master Slave flip flop.	*CO3*	*PO2*	**10**
		b)	Derive the characteristic equations of SR, D, JK and T Flip-flops.	*CO3*	*PO2*	**10**
			UNIT - IV			
	5	a)	With a neat block diagram and truth table show the operation performed by Universal Shift Register.	*CO3*	*PO2*	**10**
		b)	Define shift register. With a neat logic diagram, truth table show the working of a Johnson Counter.	*CO3*	*PO2*	**10**
			OR			
	6	a)	With a neat logic diagram and truth table, show the working of a four-bit Synchronous Binary Counter.	*CO3*	*PO2*	**10**
		b)	Design a Mod-5 synchronous counter using Negative Edge Triggered JK flip-flops.	*CO4*	*PO3*	**10**
			UNIT - V			
	7	a)	Design a Mealy Model Sequence Detector (Synchronous sequential) circuit, that outputs 1 whenever the sequence "011" occurs at its input x otherwise output y is 0.	*CO4*	*PO3*	**10**
		b)	Reduce the state transition diagram given below using: i. Row elimination method ii. Implication table method 	*CO4*	*PO3*	**10**

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