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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E.

Semester: III

Branch: Information Science and Engineering

Duration: 3 hrs.

Course Code: 23IS3PCDLD/22IS3PCDLD

Max Marks: 100

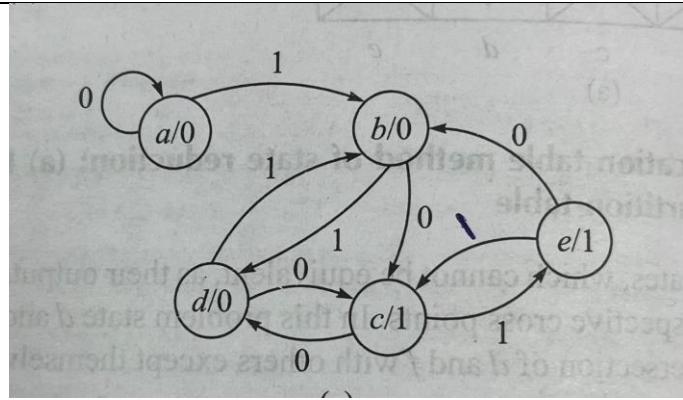
Course: Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I			CO	PO	Marks
1	a)	<p>Using K map simplify the following Boolean functions and obtain the minimal sum.</p> <p>i. $F(A, B, C, D) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$</p> <p>ii. $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$</p>	<i>CO2</i>	<i>PO1</i>	10
	b)	<p>Obtain the prime implicants and essential prime implicants using Quine-McClusky method.</p> <p>$f(a,b,c,d) = \sum m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$</p>	<i>CO3</i>	<i>PO2</i>	10
OR					
2	a)	<p>Minimize the following function for SOP using K-MAP method and implement it using basic gates.</p> <p>a. $F(A, B, C, D) = \pi M(5, 7, 13, 14, 15) + d(1, 2, 3, 9)$</p>	<i>CO2</i>	<i>PO1</i>	10
	b)	<p>Draw the truth table for the logical function M for three inputs A, B and C, where $M = F(A, B, C)$. The output is 0 (zero), if the majority of inputs are zero (0) and one (1) if the majority of inputs are one (1). Write the sum of products expression (SOP) and circuit diagram for M.</p>	<i>CO2</i>	<i>PO1</i>	6
	c)	<p>Construct truth table for each of the following Boolean functions</p> <p>i) $F(A, B, C) = (A' + B)(B' + C)$</p> <p>ii) $F(A, B, C) = AB + BC + CA$</p>	<i>CO2</i>	<i>PO1</i>	4
UNIT - II					
3	a)	<p>With a neat diagram, show the organization of a BCD adder.</p>	<i>CO2</i>	<i>PO1</i>	10
	b)	<p>Realize the following Boolean expression using</p> <p>i. An 8-to-1-line multiplexer where w, x and y appear on select lines S2, S1 and S0 respectively.</p>	<i>CO3</i>	<i>PO2</i>	10

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		<p>ii. A 4-to-1-line multiplexer where w and x appear on select lines S1 and S0 respectively. $f(w, x, y, z) = \Sigma m(0,1,5,6,7,9,12,15)$</p>			
		OR			
4	a)	With a neat logic diagram discuss the working of a 4-bit carry look ahead adder.	CO2	PO1	10
	b)	Design a 3-to-8 line decoder using two 2-to-4 line decoders.	CO2	PO1	5
	c)	Realize the Boolean expression using 4:1 where w, x appear for the select lines S ₁ , S ₀ . $f(w, x, y, z) = \Sigma m(0,1,5,6,7,9,13,14)$.	CO3	PO2	5
		UNIT - III			
5	a)	With a neat block diagram, truth table show the working of i) Gated SR flipflops ii) Gated D flipflops	CO2	PO1	10
	b)	Write the truth table, state transition diagram and excitation table of SR, D, JK flipflops.	CO2	PO1	10
		OR			
6	a)	With a neat circuit diagram and timing diagram illustrate the working of a Master Slave JK flipflop.	CO3	PO2	10
	b)	Draw the logic diagram of positive edge triggered D flip flop and discuss its working with truth table and timing diagram.	CO3	PO2	10
		UNIT - IV			
7	a)	With a neat diagram show the working of parallel-in-serial out shift register.	CO3	PO2	10
	b)	Design a 3-bit Asynchronous up counter using JK Flip flop. Show its working.	CO3	PO2	10
		OR			
8	a)	Design a self-correcting mod 5 synchronous down counter using JK Flip flop. Assume 100 as the next state for all the unused states.	CO3	PO2	10
	b)	With a neat logic diagrams truth table show the working of i) Ring Counter ii) Johnson Counter	CO3	PO2	10
		UNIT - V			
9	a)	Design a Moore model sequence detector circuit, that outputs 1 whenever the sequence "011" occurs at its input X otherwise output y is 0.	CO4	PO3	10
	b)	Reduce the state transition diagram given below using: i. Row elimination method ii. Implication table method	CO4	PO3	10



OR

10 a) Design a Mealy model sequence detector circuit, that outputs 1 whenever the sequence “011” occurs at its input X otherwise output y is 0.

CO4 PO3 10

b) Reduce the state transition diagram given below using:
i. Row elimination method
ii. Implication table method

