U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

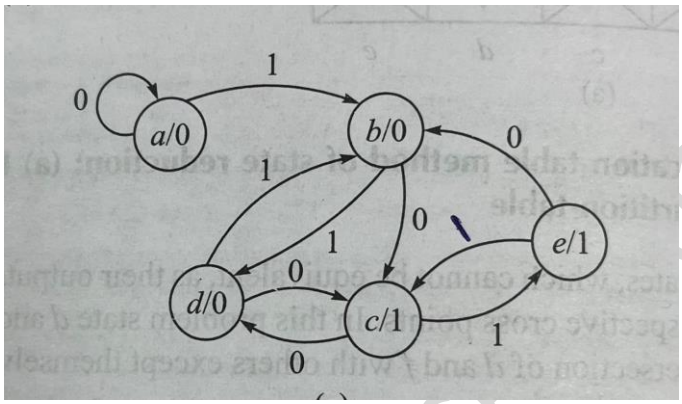
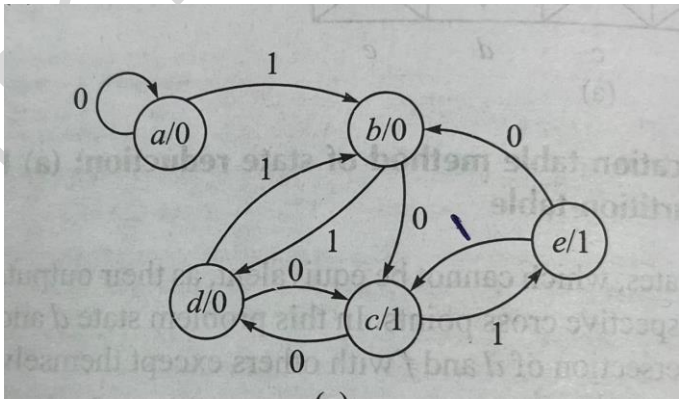
Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 23IS3PCDLD / 22IS3PCDLD / 19IS3PCDLD **Max Marks: 100**
Course: Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	For the following Boolean function F(w, x, y, z) = ∑m (2,4,6,7, 9,12,14,15) i. Write the maxterms in πM form ii. Write the minterms in algebraic form iii. Write the maxterms in algebraic form	CO2	PO2	05
	b)	Simplify the following Boolean function by using K-map method in POS form: f(A,B,C,D) = ∑m (0, 1, 2, 3, 4, 5, 7)	CO2	PO2	05
	c)	Obtain the prime implicants and essential prime implicants using Tabulation Method: $F(a,b,c,d) = \sum(0,1,2,3,4,6,7,11,12,15)$	CO2	PO2	10
		OR			
2	a)	A four-bit binary number is represented as $A_3A_2A_1A_0$, where A_3, A_2, A_1, A_0 represent the individual bits and A0 is equal to the LSB. Design a digital system that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000. i) Write the truth table ii) Using K-Map simplify the Boolean expression for SOP.	CO2	PO2	06
	b)	Using K-map, simplify the following Boolean functions. Obtain minimal sum expressions. i) f (A, B, C, D) = Σm (0,2,4,10,11,14) + d (6,7) ii) f (A, B, C, D) = Σm (2,3,8,9,10,12,13) + d (7,11)	CO2	PO1	08
	c)	Obtain prime implicants using Quine McClusky method $F(a,b,c,d) = m(0,4,8,10,12,13,15) + d(1,2)$	CO2	PO2	06

			UNIT - II			
	3	a)	Detail out the general organization and working of a carry look ahead adder with a neat diagram.	*CO1*	*PO1*	**10**
		b)	Realize the following Boolean expression using f (w, x, y, z) = ∑m (1,2,6,7,9,11,12,14,15) i. An 8-to-1-line multiplexer where w, x and y appear on select lines S2, S1 and S0 respectively. ii. A 4-to-1-line multiplexer where w and x appear on select lines S1 and S0 respectively	*CO2*	*PO2*	**10**
			OR			
	4	a)	Design half subtractor.	*CO2*	*PO2*	**05**
		b)	Implement Full adder using 3-to-8 line decoder and logic gates.	*CO2*	*PO2*	**05**
		c)	With a neat diagram, discuss the organization of a single decade BCD adder with correction logic.	*CO2*	*PO2*	**10**
			UNIT - III			
	5	a)	Differentiate between Combinational circuits and Sequential circuits.	*CO3*	*PO1*	**05**
		b)	With a neat diagram, truth table show the operation of a JK Master Slave flip flop.	*CO3*	*PO1*	**05**
		c)	Derive the characteristic equations for the given flip flops. • SR flipflop • JK Flipflop • D flipflop • T flipflop	*CO3*	*PO2*	**10**
			OR			
	6	a)	With a neat logic diagram, logic symbol, characteristic table, and timing diagram, explain the working of a positive edge triggered JK flip flop.	*CO3*	*PO2*	**10**
		b)	Draw the state transition diagram and derive the excitation table of SR, D, and JK Flip-flops.	*CO3*	*PO2*	**10**
			UNIT - IV			
	7	a)	Outline the operations performed by universal shift register. Provide details on its design with logic diagram and truth table.	*CO3*	*PO2*	**10**
		b)	Design a 3-bit asynchronous down counter.	*CO3*	*PO2*	**10**
			OR			
	8	a)	With a neat diagram show the working of SISO, SIPO shift registers.	*CO1*	*PO1*	**10**

		b)	Design a synchronous mod-10 counter using positive-edge triggered D flipflops.	*CO3*	*PO2*	**10**
			UNIT - V			
	9	a)	Design a sequence detector that receives binary data stream at its input and signals when a combination '011' arrives at the input by making its output, Y high which otherwise remains low. Consider, data is coming from left ie the first bit to be identified is 1, second 1 and third 0. Design a Moore Model along with State Transition Diagram and State Synthesis table.	*CO4*	*PO3*	**10**
		b)	Reduce the state transition diagram given below using implication table method. 	*CO4*	*PO3*	**10**
			OR			
	10	a)	Design a sequence detector that receives binary data stream at its input and signals when a combination '011' arrives at the input by making its output, Y high which otherwise remains low. Consider, data is coming from left ie the first bit to be identified is 1, second 1 and third 0. Design a Mealy Model along with State Transition Diagram and State Synthesis table.	*CO4*	*PO3*	**10**
		b)	Apply row elimination method to simplify given state diagram. 	*CO4*	*PO2*	**10**

******