U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

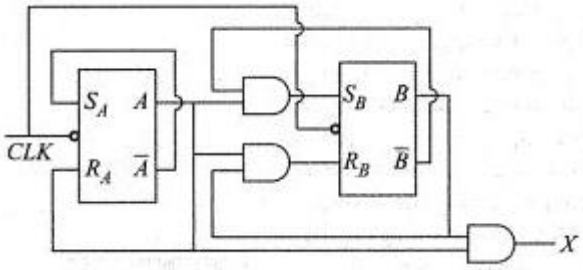
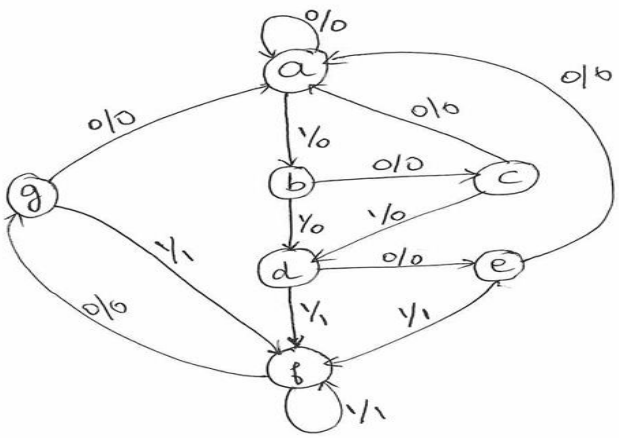
Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Information Science and Engineering **Duration: 3 hrs.**
Course Code: 23IS3PCDLD **Max Marks: 100**
Course: Digital Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	*CO*	*PO*	Marks
1	a)	A digital system of four variables (A, B, C, D) is to be designed in which the months of the year is given as input in four-bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess numbers in the input beyond '1011' as don't care conditions. • Construct the Truth Table • Write the corresponding Minterm canonical formula in • algebraic form and in ∑m-notation. • Using K-Map, Simplify the Boolean Expression for Minterm Canonical form • Implement the Simplified Equation using NAND Gate.	*C02*	*PO1*	**10**
	b)	Simplify the following Boolean Function using Tabulation Method and obtain all the Prime Implicants and Essential Prime Implicants. F(A,B,C,D) =∑m(1,2,8,9,10,12,13,14)	*C02*	*PO1*	**10**
		OR			
2	a)	Find the Minimal Sum and Minimal Product using K-Map. F(A,B,C,D) =∑m(6,7,9,10,13) +∑d(1,4,5,11)	*C02*	*PO1*	**06**
	b)	Obtain the Prime Implicants and Essential Prime Implicants using Quine-McCluskey method for the given Boolean function. F(A,B,C,D) =∑m(0,1,2,3,10,11,12,13,14,15)	*C02*	*PO1*	**10**
	c)	Define Universal Gates.Realize basic gates using Universal Gates	*C01*		**04**

			UNIT-II			
	3	a)	Implement the given Boolean Function using 8:1 MUX where x,y,z appears on the select lines S_2,S_1,S_0. $F(w,x,y,z) = \sum m(0,4,6,8,9,11,13,14)$	*CO3*	*PO2*	**07**
		b)	Design 2-bit Comparator using Logic Gates	*CO3*	*PO2*	**07**
		c)	Realize the given Boolean Expressions using 3:8 line decoder and a NOR gate. $F_1(x_2,x_1,x_0) = \sum m(0,1,5,6,7)$ & $F_2(x_2,x_1,x_0) = \sum m(1,2,3,6,7)$	*CO3*	*PO2*	**06**
			UNIT - III			
	4	a)	With a neat block diagram, Illustrate the working of a Master-Slave JK Flip-Flops along with its Truth-Table.	*CO3*	*PO2*	**08**
		b)	Analyze the given Sequential Circuit with the help of State Table and State Transition Diagram. 	*CO4*	*PO3*	**08**
		c)	Show the Characteristic Equations of JK and D-Flip-flops	*CO2*	*PO1*	**04**
			UNIT-IV			
	5	a)	With a neat diagram Illustrate a 4-bit Universal Shift Register.	*CO2*	*PO1*	**10**
		b)	Design a Synchronous Mod-6 counter using JK Flip-Flop.	*CO4*	*PO3*	**10**
			OR			
	6	a)	Design and implement a MOD-5 Synchronous Counter using JK flip-flops.	*CO4*	*PO3*	**10**
		b)	With a neat diagram show the working of Parallel In Serial Out Shift Register.	*CO2*	*PO1*	**10**
			UNIT - V			
	7	a)	Reduce the given State Transition Diagram by Row Elimination Method. 	*CO4*	*PO3*	**06**

		b)	Design a sequence detector that receives binary data stream at its input,X and signals when a combination '011' arrives at the input by making its output, Y high which otherwise remains low. Consider, data is coming from left ie the first bit to be identified is 1, second 1 and third 0. Design a Moore Model along with State Transition Diagram and State Synthesis table.	*CO4*	*PO3*	**10**
		c)	Illustrate with a diagram the differences between Moore and Mealy Model.	*CO2*	*PO1*	**04**

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