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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Medical Electronics Engineering **Duration: 3 hrs.**

Course Code: 23MD5PE1DV **Max Marks: 100**

Course: Digital System Design Using Verilog

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	With necessary block diagram, explain different design methodologies in digital design. Also show the design hierarchy for ripple carry counter using its building blocks.	*CO1*	*PO1*	**10**
	b)	Along with example, illustrate Verilog ports.	*CO1*	*PO1*	**10**
		OR			
2	a)	Explain Verilog data types with an example for each.	*CO1*	*PO1*	**10**
	b)	Perform the following operations If A = 1101010, B = 1011010, C = 1010 i. Y1 = {C, B, A} ii. Y2 = A^ B iii. Y3 = A>>3 iv. Y4 = ~ (&B) v. Y5 = A&(~B) vi. Y6 = A~^B	*CO1*	*PO1*	**10**
		UNIT - II			
3	a)	Develop Verilog code for 4:1 MUX using (i) Conditional operator (ii) Structural modeling.	*CO2*	*PO2*	**12**
	b)	Develop Verilog code for half adder.	*CO1*	*PO1*	**08**
		OR			
4	a)	Design and hence write the Verilog code for 2-bit X 2-bit Combinational Array Multiplier.	*CO2*	*PO2*	**10**
	b)	Develop Verilog code for full subtractor using structural modeling.	*CO2*	*PO2*	**10**

			UNIT - III			
	5	a)	Develop Verilog code for (i) 8:1 MUX (ii) 2:4 decoder using behavioral modeling.	*CO2*	*PO2*	**10**
		b)	Develop Verilog code for (i) D FF (ii) T FF.	*CO2*	*PO2*	**10**
			OR			
	6	a)	Develop Verilog code for (i) 4:2 priority encoder (ii) 4-bit comparator using behavioral modeling.	*CO2*	*PO2*	**10**
		b)	Differentiate between 'always' and 'initial' statements used in behavioral modeling with an example for each.	*CO1*	*PO1*	**10**
			UNIT - IV			
	7	a)	What is an FSM. Differentiate between the different models.	*CO3*	*PO3*	**10**
		b)	Design "101" sequence detector with overlapping using Mealy FSM.	*CO3*	*PO3*	**10**
			OR			
	8	a)	Write a Verilog code to implement 3 bit Binary to Gray code conversion.	*CO3*	*PO3*	**10**
		b)	Design a sequence detector to detect the sequence "1111" (overlapped) and describe the Verilog behavior.	*CO3*	*PO3*	**10**
			UNIT - V			
	9	a)	Implement the functions f1 and f2 using PLA. f1 = Σm (1,2,3,7) f2 = Σm (0,1,2,6).	*CO3*	*PO3*	**12**
		c)	Differentiate digital design implementation using FPGA and CPLD with necessary examples.	*CO1*	*PO1*	**08**
			OR			
	10	a)	With a neat diagram analyse the CPLD implementation.	*CO1*	*PO1*	**10**
		b)	Differentiate between CPLDs, FPGA, and ASIC in terms of design implementation.	*CO1*	*PO1*	**10**

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