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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Medical Electronics Engineering **Duration: 3 hrs.**

Course Code: 23MD5PE1DV **Max Marks: 100**

Course: Digital System Design Using Verilog

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		With the help of a flow chart, explain the typical Design flow in Verilog for designing VLSI IC circuits	CO1	PO1	**10**
	b)		Discuss briefly the 4 levels of abstraction in digital design.	CO1	PO1	**10**
			OR			
2	a)		Explain the different design methodologies employed in Verilog. Give their merits and demerits.	CO1	PO1	**10**
	b)		Explain all the available data types in Verilog with examples.	CO1	PO1	**10**
			UNIT - II			
3	a)		Write a dataflow description in Verilog for a 3-bit carry look ahead adder.	CO2	PO2	**08**
	b)		Design and write a structural code for a full adder by taking half adder instances in the main module. Write the lower-level module using dataflow description.	CO2	PO2	**12**
			OR			
4	a)		Write a Verilog code to implement a half subtractor.	CO2	PO2	**10**
	b)		Write a Verilog code for 2 to 4 decoder using dataflow and gate level descriptions.	CO2	PO2	**10**
			UNIT - III			
5	a)		What are the different procedural assignment statements used in Verilog? With an appropriate example, bring out their differences?	CO3	PO3	**10**
	b)		Write a Verilog behavioral description to implement SR flip-flop.	CO3	PO3	**10**
			OR			

	6	a)	Write a Verilog behavioral description to implement JK- flip-flop.	CO3	PO3	**10**
		b)	Explain the following control statement with an example i)if…. else statement ii) for loop	CO1	PO1	**10**
			UNIT - IV			
	7	a)	With neat blocks diagrams explain the different types of FSM?	CO1	PO1	**10**
		b)	Draw the state level diagram and develop the Verilog RTL for an overlapping Moore state machine which produces output as '1' if the input bit stream is "101" with neat indentation, comments and header.	CO3	PO3	**10**
			OR			
	8	a)	Draw the state level diagram and develop the Verilog RTL for an overlapping Moore state machine which produces output as '1' if the input bit stream is "101" with neat indentation, comments and header.	CO3	PO3	**10**
		b)	Write a Verilog code to implement 3 bit Binary to Gray code conversion.	CO2	PO2	**10**
			UNIT - V			
	9	a)	What are PAL devices? With neat diagrams, explain the architecture of any CPLD.	CO1	PO1	**10**
		b)	Implement the functions f1 and f2 using PLA of appropriate size. f1 = Σm (1,2,3,7) f2 = Σm (0,1,2,6). Draw PLA Table.	CO3	PO3	**10**
			OR			
	10	a)	What is the role of FPGAs in ASIC market? Write a note on FPGA technologies.	CO1	PO1	**10**
		b)	Compare the following: CPLDS, FPGA and ASIC.	CO1	PO1	**10**

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