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B.M.S. College of Engineering, Bengaluru-560019

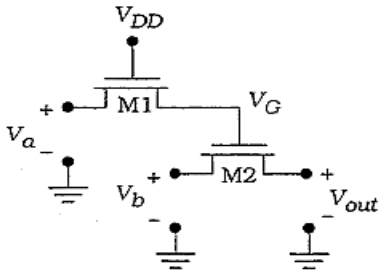
Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Medical Electronics Engineering **Duration: 3 hrs.**
Course Code: 22MD5PE1VL **Max Marks: 100**
Course: VLSI DESIGN

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Design a CMOS logic Gate for the function: $f(a,b,c) = \overline{a.(b+c)}$ using minimum number of transistors.	CO1	PO1	**08**
	b)	Design the following using 8:1 MUX: i) CMOS NAND3 gate ii) CMOS NOR3 gate	CO1	PO1	**06**
	c)	Discuss why PMOS transistors are often preferred for implementing logic 1, while NMOS transistors are favored for logic 0.	CO1	PO1	**06**
		OR			
2	a)	The output of a nFET is used to drive the gate of another nFET as shown in Fig.2a Assume that $V_{DD} = 3.3V$ and $V_{Th} = 0.6$ V. Find the output voltage V_{out} when the input voltages are at the following values: i) $V_a = 3.3$ V and $V_b = 3.3$ V ii) $V_a = 0.5$ V and $V_b = 3.0$ V iii) $V_a = 2.0$ V and $V_b = 2.5$ V iv) $V_a = 3.3$ V and $V_b = 1.8$ V  Fig.2a	CO2	PO3	**08**
	b)	Consider two input XOR function a ⊕ b to design: i) XOR gate using 4:1 MUX ii) 2 input XNOR by modifying the circuit. iii) A full adder with inputs a, b, c to calculate the sum bit, **S = a ⊕ b ⊕ c**	CO2	PO3	**08**
	c)	Explain AND & OR logic operation using assert high switches and verify the truth table.	CO1	PO1	**04**

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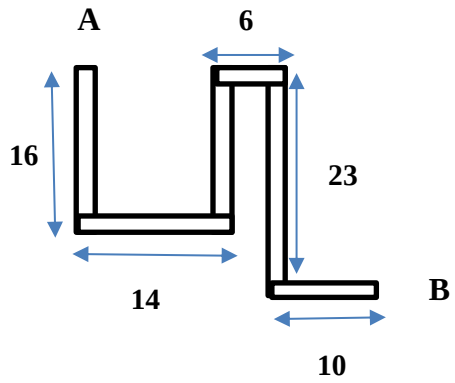
			UNIT - II			
	3	a)	Derive the relationship between sheet resistance and line resistance, emphasizing how sheet resistance influences the overall line resistance. For the interconnect pattern shown in Fig. 3a, the line has a width of 1 Unit and the sheet resistance is R_s = 25Ω. Find the resistance from A to B if each corner square contributes a factor of 0.625 of a "straight-path" square.  Fig.3a	*CO3*	*PO2*	**08**
		b)	A sample of silicon is doped with Arsenic with $N_d = 4x10^{17}$ cm^{-3}. i) Find the majority carrier density ii) Find the minority carrier density iii) Calculate the electron and hole mobilities and then find the conductivity of the sample.	*CO3*	*PO2*	**06**
		c)	Define Euler graph and outline the key characteristics using an example.	*CO3*	*PO2*	**06**
			OR			
	4	a)	Consider the logic function F = not(a+b.c) Design the CMOS logic gate and layout that provides this function.	*CO2*	*PO3*	**07**
		b)	Describe the primary layers found in a CMOS integrated circuit, including the semiconductor substrate, gate oxide, polysilicon, and metal layers. What is the function of each layer?	*CO2*	*PO3*	**06**
		c)	Describe the factors that influence the layout geometry of CMOS gates, including transistor sizing, spacing, and interconnect routing.	*CO2*	*PO3*	**07**
			UNIT - III			
	5	a)	Describe the typical DC voltage transfer characteristics (VTC) of a CMOS inverter, highlighting the key regions and important voltage levels.	*CO3*	*PO2*	**08**
		b)	Find the ratio β_n / β_p needed to obtain an inverter midpoint voltage of $\mathbf{V_M = 1.3V}$ with a power supply of 3V. Assume that $\mathbf{V_{Tn} = 0.6}$ **V** and $\mathbf{V_{Tp} = -0.82}$ **V**. What would be the relative device sizes if $\mathbf{K'_n = 110uA/V^2}$ and the mobility values are related by $\mathbf{\mu_n = 2.2\ \mu_p}$?	*CO3*	*PO2*	**06**

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		c)	Discuss the voltage transfer characteristics (VTC) of a CMOS NAND2 gate and derive the expression for V_M for the case of simultaneous switching.	*CO3*	*PO2*	**06**
			OR			
	6	a)	Identify the sources of power dissipation in a CMOS invertor. Justify your answer to say the dynamic and static power dissipation differs from each other.	*CO3*	*PO2*	**07**
		b)	What role does parasitic capacitance play in the DC characteristics and switching behavior of CMOS gates? Discuss its impact on performance.	*CO3*	*PO2*	**07**
		c)	With proper analysis prove k`n/k`p=μn/μp=r.	*CO3*	*PO2*	**06**
			UNIT - IV			
	7	a)	Explain the role of sheet resistance in the MOS transistors within a CMOS inverter by using a formula for channel resistance.	*CO4*	*PO4*	**06**
		b)	Discuss the significance of area capacitance in the performance of integrated circuits and derive the formula for calculating area capacitance.	*CO4*	*PO4*	**08**
		c)	Describe about the methods for driving large capacitive loads.	*CO4*	*PO4*	**06**
			OR			
	8	a)	Estimate the rise time and fall time delay of a CMOS inverter using appropriate circuit model.	*CO4*	*PO4*	**08**
		b)	Evaluate the propagation delay through the cascaded pass transistors network.	*CO4*	*PO4*	**06**
		c)	Explain the electrical constraints that play a crucial role in determining the appropriate layers in CMOS technology	*CO4*	*PO4*	**06**
			UNIT - V			
	9	a)	Explain the primary scaling factors and their effect on various key parameters of MOS FET devices	*CO4*	*PO4*	**08**
		b)	Discuss on the role of interconnect and contact resistance play in influencing the performance and scalability of CMOS circuits	*CO4*	*PO4*	**06**
		c)	Illustrate the nature of and approach to structured design using parity generator as an example.	*CO4*	*PO4*	**06**
			OR			
	10	a)	Discuss the limitations of scaling (any three)	*CO4*	*PO4*	**06**
		b)	Analyze the guidelines to be followed for large system designs in MOS technology.	*CO4*	*PO4*	**06**
		c)	Discuss how layout techniques (e.g., floorplanning, routing) are impacted by scaling. What design rules become critical in high-density layouts?	*CO4*	*PO4*	**08**

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