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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Medical Electronics Engineering **Duration: 3 hrs.**

Course Code: 22MD5PE1VL **Max Marks: 100**

Course: VLSI Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Review the pass characteristics of nFET and pFET .	CO3	PO2	**06**
	b)		Design a transmission gate based 2-to-1 multiplexer.	CO1	PO1	**06**
	c)		Discuss the different levels of design representation.	CO1	PO1	**08**
			OR			
2	a)		When would you select MOS or BJT for your application? Justify your choice.	CO1	PO1	**06**
	b)		Design a CMOS circuit to implement the following Boolean expressions i)$f = \overline{a.(b+c)}$ ii) $f = \overline{a.b + a.c + b.d}$	CO2	PO3	**06**
	c)		Summarize the physical device cycle with a neat flowchart.	CO1	PO1	**08**
			UNIT - II			
3	a)		Specify the significance of Euler graph and illustrate .	CO3	PO2	**10**
	b)		Identify the role of MOSFET layers in a N-well process.	CO2	PO3	**10**
			OR			
4	a)		Discuss the physical structure of MOSFET with relevant figures.	CO1	PO1	**08**
	b)		State few rules about the stick diagram and sketch the stick diagram for CMOS inverter.	CO3	PO2	**12**
			UNIT - III			
5	a)		Derive the expression for power dissipation of a CMOS inverter.	CO2	PO3	**08**
	b)		Discuss the switching characteristics of two input NAND gate.	CO3	PO2	**12**

			OR			
	6	a)	Explain the DC characteristics of CMOS inverter.	*CO3*	*PO2*	**12**
		b)	Specify the rise and fall time of a pass transistor.	*CO3*	*PO2*	**04**
		c)	Depict the DC and transient analysis of a CMOS circuit.	*CO3*	*PO2*	**04**
			UNIT - IV			
	7	a)	Define Standard capacitance □**C**g and calculate its value for i)5μm MOS circuit with gate capacitance value of $4x10^{-4}$ pF/ μm^2 ii) 1.2μm MOS circuit with gate capacitance value of $16x10^{-4}$ pF/ μm^2	*CO4*	*PO4*	**05**
		b)	Explain the concept of driving large capacitive loads using cascaded inverters.	*CO4*	*PO4*	**09**
		c)	Identify and explain the constraints that should be considered while choosing the layers.	*CO4*	*PO4*	**06**
			OR			
	8	a)	Derive the expression for sheet resistance $\mathbf{R_s}$	*CO4*	*PO4*	**05**
		b)	Calculate the total delay for a pair of i)NMOS inverters ii)CMOS inverters	*CO4*	*PO4*	**10**
		c)	Illustrate the resistance calculation for the transistor channel.	*CO4*	*PO4*	**05**
			UNIT - V			
	9	a)	What are the advantages of scaling in VLSI technology? Explain different scaling models with scaling factors.	*CO4*	*PO4*	**10**
		b)	Explain the limitation of scaling on i) Miniaturization ii) Interconnect & contact resistance.	*CO4*	*PO4*	**10**
			OR			
	10	a)	Explain the different types of scaling models with derivation for channel resistance and gate delay.	*CO4*	*PO4*	**10**
		b)	Summarize the guidelines that need to be followed to have a good system design.	*CO4*	*PO4*	**10**

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