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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

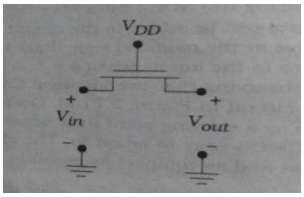
Branch: Medical Electronics Engineering **Duration: 3 hrs.**

Course Code: 23MD6PE2VD **Max Marks: 100**

Course: VLSI Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	With a neat diagram explain the CMOS NOR2 gate functionality.	*CO1*	*PO1*	**06**
	b)	Design a TG-based 2-to-1 multiplexor and explain its working.	*CO1*	*PO1*	**06**
	c)	Consider the 2-input XOR function a XOR b. i) Design an XOR gate using a 4:1 MUX. ii) Modify the circuit in (i) to produce a 2-input XNOR. iii) A full adder accepts inputs a, b and c and calculates the sum bit s=a XOR b XOR c. Use MUX-based gates to design a circuit with this output.	*CO1*	*PO1*	**08**
		OR			
2	a)	Design a CMOS logic gate for the function F=not (a.b+a.c+b.d) using minimal transistor count.	*CO1*	*PO1*	**06**
	b)	Design a 4:1 MUX using three 2:1 TG multiplexers.	*CO1*	*PO1*	**06**
	c)	Suppose that V_{DD} = 5 V and V_{Tn} = 0.7 V. Find the output voltage V_{out} of the nFET in Figure 2.c for the following input voltage values: i) Vin = 2 V ii) Vin = 4.5 V iii) Vin = 3.5 V iv) Vin = 0.7 V  Figure 2.c	*CO1*	*PO1*	**08**

			UNIT - II			
	3	a)	Consider the logic function F = not(a+b.c) Design the CMOS logic gate and layout that provides this function.	*CO2*	*PO3*	**08**
		b)	An interconnect line runs over an insulating oxide layer that is 10,000 Å thick. The line has a width of 0.5 μm and is 40 μm long.The sheet resistance is known to be 25Ω. i) Find the line resistance. ii) Find the line capacitance. Use €ox=3.453x10/13 F/cm, and express your answer in femto farads where 1fF=10/15F.	*CO2*	*PO3*	**06**
		c)	Construct the Euler's graph for the function g = not (a+b.c).	*CO2*	*PO3*	**06**
			OR			
	4	a)	Describe the primary layers found in a CMOS integrated circuit, including the semiconductor substrate, gate oxide, polysilicon, and metal layers. What is the function of each layer?	*CO2*	*PO3*	**06**
		b)	Describe the factors that influence the layout geometry of CMOS gates, including transistor sizing, spacing, and interconnect routing.	*CO2*	*PO3*	**07**
		c)	Describe the process of constructing an Euler graph from a circuit netlist. How are nodes and edges represented?	*CO2*	*PO3*	**07**
			UNIT - III			
	5	a)	With neat sketches explain the voltage transfer curve for the NOT gate.	*CO3*	*PO2*	**06**
		b)	With neat diagram explain the NAND2 VTC analysis along with the transition table.	*CO3*	*PO2*	**07**
		c)	With proper analysis prove k`n/k`p=μn/μp=r.	*CO3*	*PO2*	**07**
			OR			
	6	a)	Draw and explain the DC transfer characteristics of a CMOS NAND gate.	*CO3*	*PO2*	**06**
		b)	What role does parasitic capacitance play in the DC characteristics and switching behavior of CMOS gates? Discuss its impact on performance.	*CO3*	*PO2*	**07**
		c)	Identify the sources of power dissipation in a CMOS inverter. How do dynamic and static power dissipation differ?	*CO3*	*PO2*	**07**
			UNIT - IV			
	7	a)	With a neat sketch derive the sheet resistance equation and give two reasons about its importance.	*CO3*	*PO2*	**07**
		b)	With simple analysis estimate the rise-time for a CMOS inverter.	*CO3*	*PO2*	**07**
		c)	Discuss the ways to route data and control signals for choice between the layers.	*CO3*	*PO2*	**06**
			OR			
	8	a)	With simple analysis estimate the fall-time for a CMOS inverter.	*CO3*	*PO2*	**07**
		b)	Calculate the delay for driving large capacitive loads.	*CO3*	*PO2*	**07**

		c)	Discuss on the design of long polysilicon wires.	*CO3*	*PO2*	**06**
			UNIT - V			
	9	a)	Calculate the effects of scaling for gate area, gate capacitance, parasitic capacitance, channel resistance and gate delay.	*CO4*	*PO4*	**10**
		b)	Discuss the limitations of scaling (Any two).	*CO4*	*PO4*	**05**
		c)	Analyze the guidelines to be followed for large system designs in MOS technology.	*CO4*	*PO4*	**05**
			OR			
	10	a)	Describe the significance of scaling factors (e.g., ℓ, W, V, and I) in the context of MOSFET performance. How can these factors be mathematically expressed for both the constant-field and constant-voltage scaling?	*CO4*	*PO4*	**07**
		b)	Explain how process variations and device matching become critical challenges as MOS devices are scaled down. How do these variations affect circuit performance?	*CO4*	*PO4*	**07**
		c)	Discuss how layout techniques (e.g., floorplanning, routing) are impacted by scaling. What design rules become critical in high-density layouts?	*CO4*	*PO4*	**06**

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