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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: MEDICAL ELECTRONICS ENGINEERING **Duration: 3 hrs.**
Course Code: 19ML5PE2DV **Max Marks: 100**
Course: Digital System Design using Verilog **Date: 03.03.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Discuss the VLSI design flow starting from design idea upto fabrication of a chip. **06**

b) With truth tables, explain the following Verilog primitives: **08**

(i) bufif0 (ii) nor (iii) xor (iv) notif1

c) In the Verilog code, find the values of f1, f2 and f3: **06**

```
wire [7:0] a, b, c; wire f1, f2, f3;
assign a=4'b0111;
assign b=4'b1100;
assign c=4'b0100;
assign f1= ^ a;
assign f2= &(a^b);
assign f3=^a&~ ^b;
```

UNIT - II

2 a) Define a parameterized parity module that takes input as a vector whose size is set by the parameter. The module has a single output which is "1" if the number of 1's in the input vector is odd and "0" otherwise. Write a dataflow Verilog code for same. **04**

b) Design a burglar alarm system with specification as, the alarm will sound if and only if the power of the alarm system is turned ON, and either a window or door has been opened. Also, the alarm should open if a door and window are both open. Also write a Verilog code for same using dataflow modeling. (Use Bitwise operator). **06**

c) Using Verilog gate-primitives, develop a Verilog structural model for the 4:1 multiplexer (with "a" as 4 bit input "sel" as selection lines and y as output). Design 16:1 multiplexer (with "a" as 16-bit input "sel" as selection lines and y as output) using 4:1 multiplexer and write Verilog code for same. **10**

OR

3 a) Design and write VERILOG code to implement the functionality of a 1-Bit comparator. **05**

b) What function do the following module implement? Justify. **10**

(i) input [31:0] x;
input [0:4] y;
input sel;
output z;
assign z = sel ? x[y] : 1'b0;

(ii) assign d = ~(c & b);
assign c = ~(a & d);

(iii) assign p = q[r];

(iv) assign q[r] =p;
where "p", "q" and "r" are variables.

c) For the following Verilog code segment, if the initial value of "Din" is 16'hCAFE, the value of "Dout" in decimal will be …… (Note that "Dout" is a 4-bit variable) **05**

```
wire [16:0] Din;
reg [3:0] DOUT;
reg [15:8] d1;
reg [7:0] d2;
always @(Din)
begin
d1 = Din [7:0];
d2 = Din [15:8];
Dout = d1[15:12] ^ d2[7:4] ^ d1[11:8];
end
```

UNIT - III

4 a) What does $display, $monitor, $finish and $stop statements specify in Verilog? **06**

b) Derive the advantage and disadvantage of using continuous assignment statement in a Verilog module with an example. **04**

c) Write a Verilog code for all the gates in different modules (any 5). **10**

OR

5 a) Develop a Verilog code for 8:3 priority encoder using behavior modelling and write test bench for the same. **10**

b) Design and write VERILOG codes to implement the functionality for **10**
i) JK Flip Flop ii) D Flipflop.

UNIT - IV

6 a) Design a serial adder circuit that adds two 12-bit numbers, A and B. The adder uses only two 12-bit shift register to store data as well as sum. Write Verilog code for the complete design. **10**

b) Design and write VERILOG code to implement the functionality of a 4-bit Gray code to Binary code convertor. **10**

UNIT - V

7 a) Explain the different types of PLDs. **10**

b) What is FPGA? Explain the different components of FPGA. **10**

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