U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: VI**
Branch: Medical Electronics Engineering **Duration: 3 hrs.**
Course Code: 19ML6PE3VS **Max Marks: 100**
Course: VLSI and SoC Design **Date: 12.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1	a)	Illustrate different threshold voltage levels related to NFET and PFET.	**08**
	b)	Demonstrate the use of complementary FET's in VLSI logic circuit designing.	**04**
	c)	Implement CMOS logic gate for the following	**08**
		i. $\overline{(a.b)+(c.d)}$ **ii.** $\overline{(a+b)}$	

UNIT - II

2	a)	Derive the expression for conductivity of semiconductor materials from the basics of physics.	**06**
	b)	With neat diagram explain the working of n-MOS transistor.	**06**
	c)	Translate the schematic circuit of CMOS Inverter into layout.	**08**

UNIT - III

3	a)	Discuss the DC characteristics of the CMOS inverter and also the voltage noise margins of the inverter.	**10**
	b)	Derive the expression of Static and dynamic power dissipation of CMOS inverter.	**10**

OR

4	a)	Outline the switching characteristics of a inverter along with the parasitic of the MOSFETS.	**10**
	b)	Derive the expression of the propagation delay of CMOS Inverter from the basics of switching activity using rise and fall times.	**10**

UNIT - IV

5	a)	State Moore's law and illustrate the advantages of the same beyond Integrated Circuits.	**05**
	b)	Illustrate the benefits of SOC with respect to Cost, Power and Performance.	**09**
	c)	Describe different IP core variants on an SOC.	**06**

OR

6	a)	Outline the comparative understanding of SOC, SOB and SOP along with relevant diagrams.	**10**
	b)	Explain the following system technologies along with relevant diagrams. i. Multichip Module (MCM) ii. Stacked IC's and Packages (SIP)	**10**

UNIT - V

7	a)	Explain canonical SOC Design flow.	**10**
	b)	Analyze the comparative understanding of top-down and bottom-up design approach of the SOC.	**10**

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