U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

July 2023 Semester End Main Examinations

Programme: B.E. **Semester: VI**
Branch: Medical Electronics Engineering **Duration: 3 hrs.**
Course Code: 19ML6PE3VS **Max Marks: 100**
Course: VLSI and SoC Design **Date: 17.07.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Describe the functions of MOSFETs as a Switch.	*CO1*	*PO1*	**05**
	b)	Explain the working of a Complementary Metal Oxide Semiconductor (CMOS) Inverter and NOR gate.	*CO2*	*PO2*	**10**
	c)	Implement XOR gate logic using Transmission gate.	*CO3*	*PO3*	**05**
		UNIT - II			
2	a)	Describe the layers used to create MOSFET with suitable diagram.	*CO2*	*PO2*	**06**
	b)	Design a CMOS circuit for 4input AOI expression F=$\overline{x.y+z.w}$	*CO3*	*PO3*	**04**
	c)	With cross-sectional view, Illustrate CMOS device with MOSFETs layers in an n-well process on p substrate.	*CO2*	*PO2*	**10**
		UNIT - III			
3	a)	Derive an Expression for Drain current flowing in a MOSFET.	*CO2*	*PO2*	**10**
	b)	With suitable circuit diagram and graphs, Analyze the Transient characteristics of CMOS Inverter circuit.	*CO3*	*PO3*	**10**
		OR			
4	a)	Derive an expression for total dynamic power dissipation in a network consisting of N number of gates.	*CO2*	*PO2*	**10**
	b)	Discuss the transient response of a 2input NAND gate.	*CO2*	*PO2*	**10**
		UNIT - IV			
5	a)	Define SOC. Discuss and Compare SOC, SIP and SOB.	*CO1*	*PO1*	**10**
	b)	What is the significance of 'reusable macros' (IP) in the designing of SOC? Explain various types of reusable macros (IP) used in SOC.	*CO2*	*PO2*	**10**

			OR			
	6	a)	Define the term "Design productivity gap". Also discuss the effect of this on time to market with suitable graph.	*CO2*	*PO2*	**10**
		b)	Define Moore's law. Elaborate on the limitations imposed by small device geometrics?	*CO2*	*PO2*	**10**
			UNIT - V			
	7	a)	With the help of neat diagram, Explain the principle of Waterfall design flow used in SOC.	*CO2*	*PO2*	**10**
		b)	Explain the system design process in detail.	*CO2*	*PO2*	**10**

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